

# COMPAL CONFIDENTIAL

MODEL NAME : *Abacus-MT*

COMPAL P/N :

PCB NO : *LA-1682*

Revision : *0.2*

## Abacus-MT Schematics Document uFCBGA/uFCPGA NorthWood MT

2003-02-25

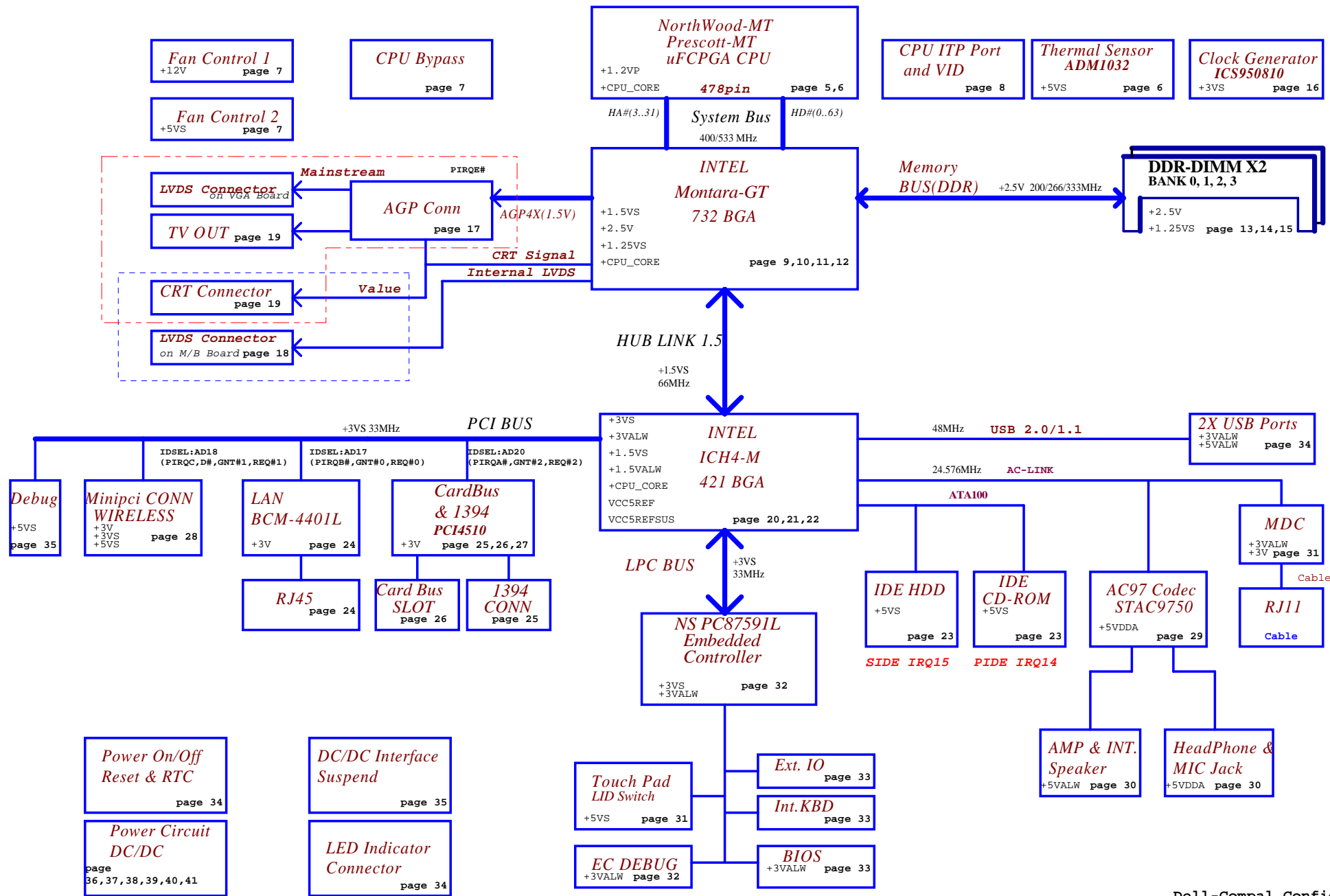
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Title		
Cover Sheet		
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Model : Abacus-MT



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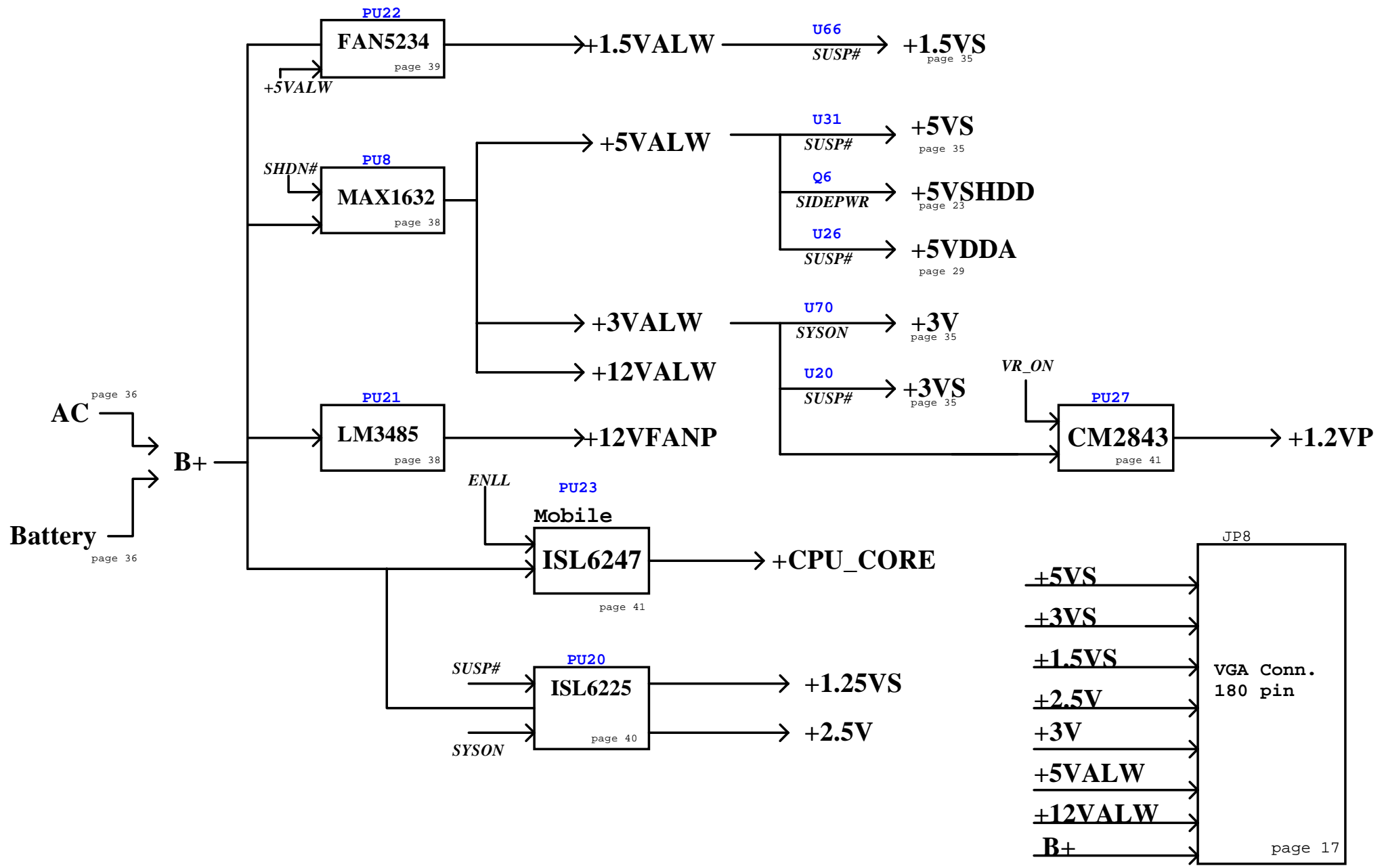
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Block Diagram

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Title		
Block Diagram		
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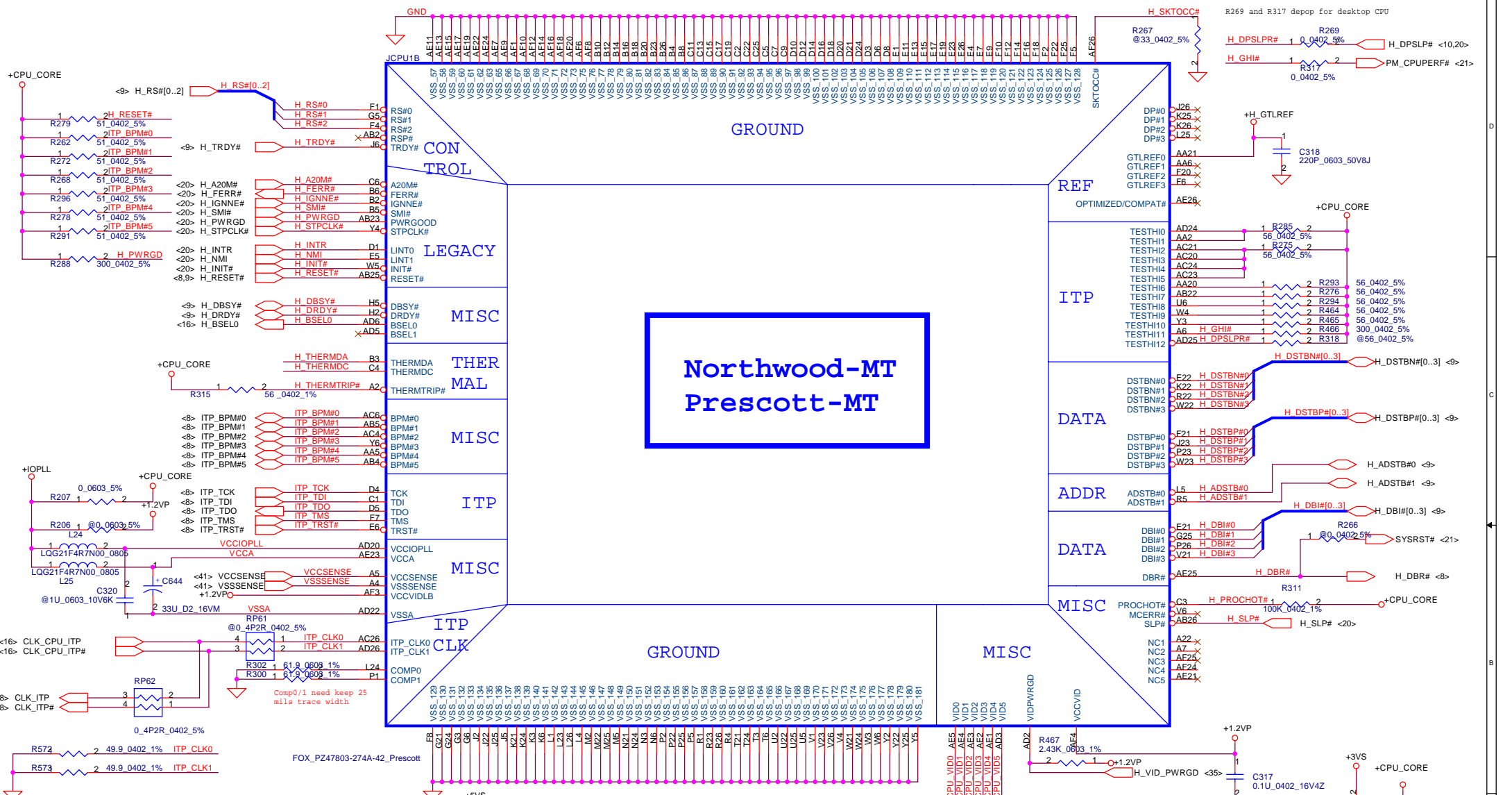
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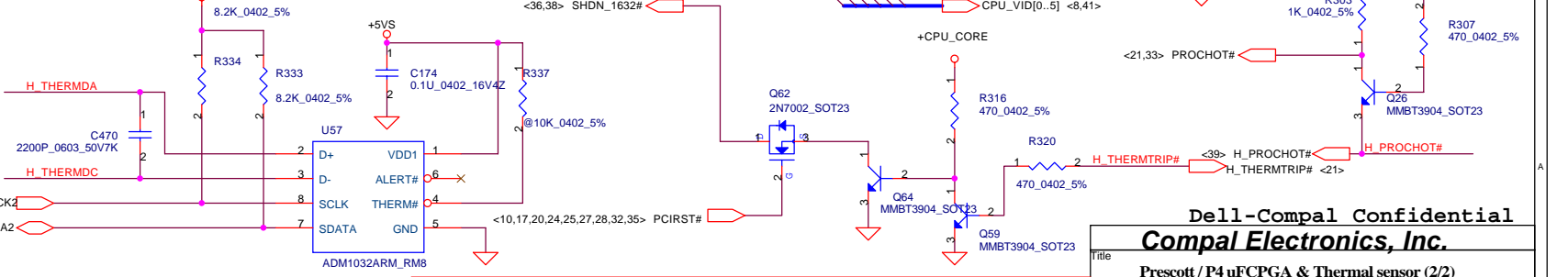
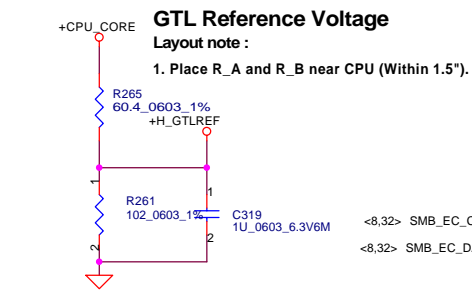
Title <b>POWER DIAGRAM</b>		
Size	Document Number <b>Abacus-MT LA-1682</b>	Rev 0.2
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# Northwood-MT Prescott-MT



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Prescott / P4 uFCPGA & Thermal sensor (2/2)		
Title	Prescott / P4 uFCPGA & Thermal sensor (2/2)	
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Intel change to 0.63VCC, then 60.4/102

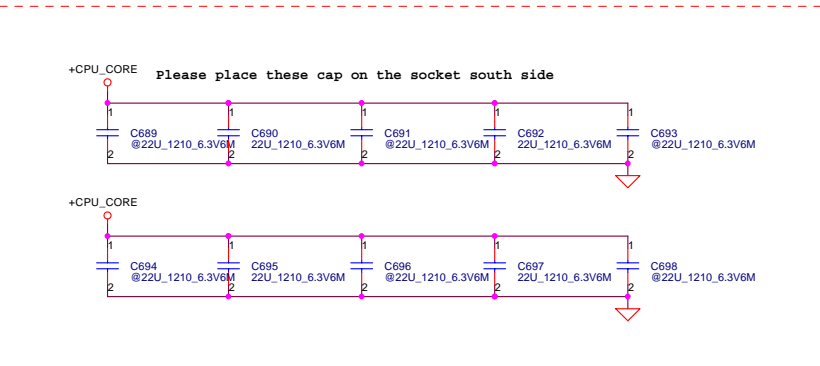
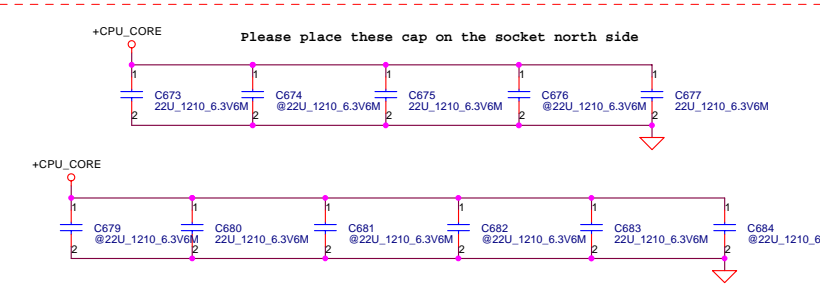
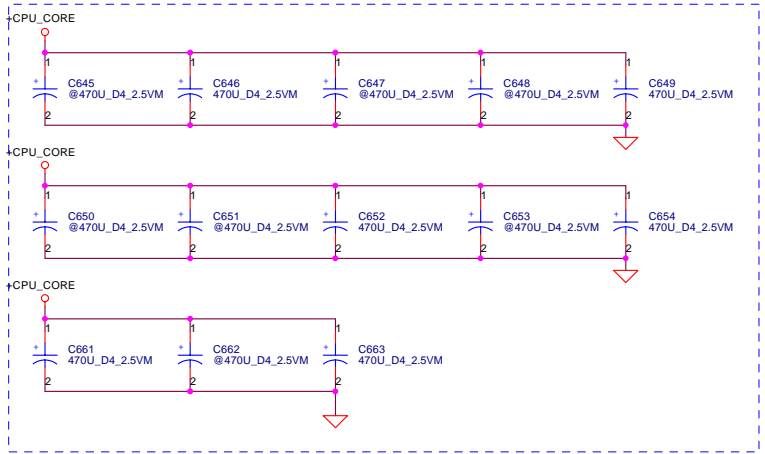
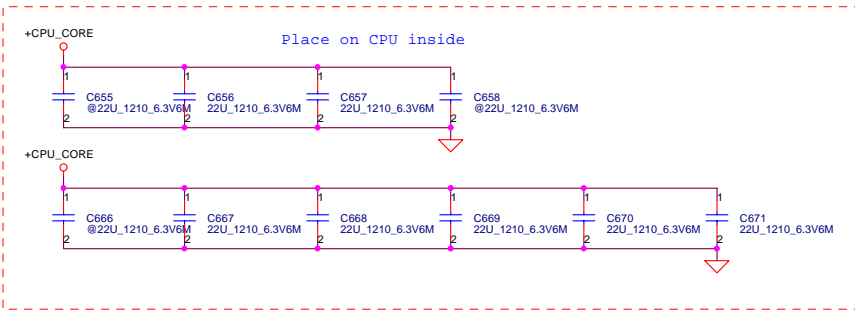
## CPU Temperature Sensor

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**Layout note :**  
Place close to CPU. Use 2-3 vias per PAD.  
Place 22uF caps x31 pcs, populated 14pcs.

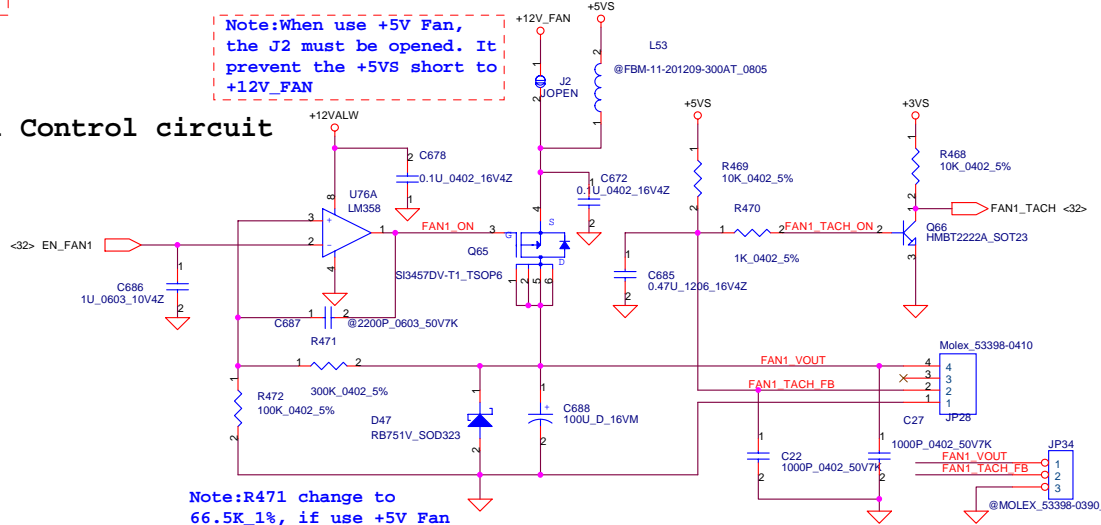
**Layout note :**  
Place close to CPU power and ground pin as possible (<1inch)

**For Desktop's CPU:**  
470uF x 15/10m ohm each  
Total 0.67m ohm



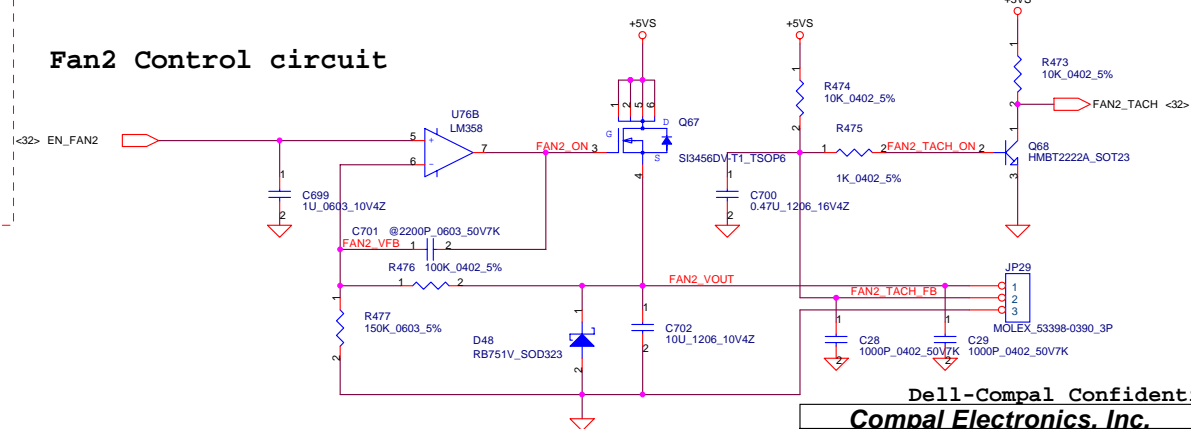
Note: When use +5V Fan, the J2 must be opened. It prevent the +5VS short to +12V\_FAN

**Fan1 Control circuit**



Note: R471 change to 66.5K\_1%, if use +5V Fan

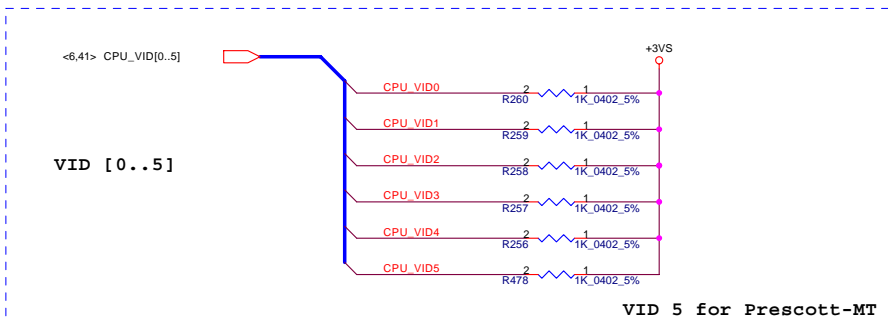
**Fan2 Control circuit**



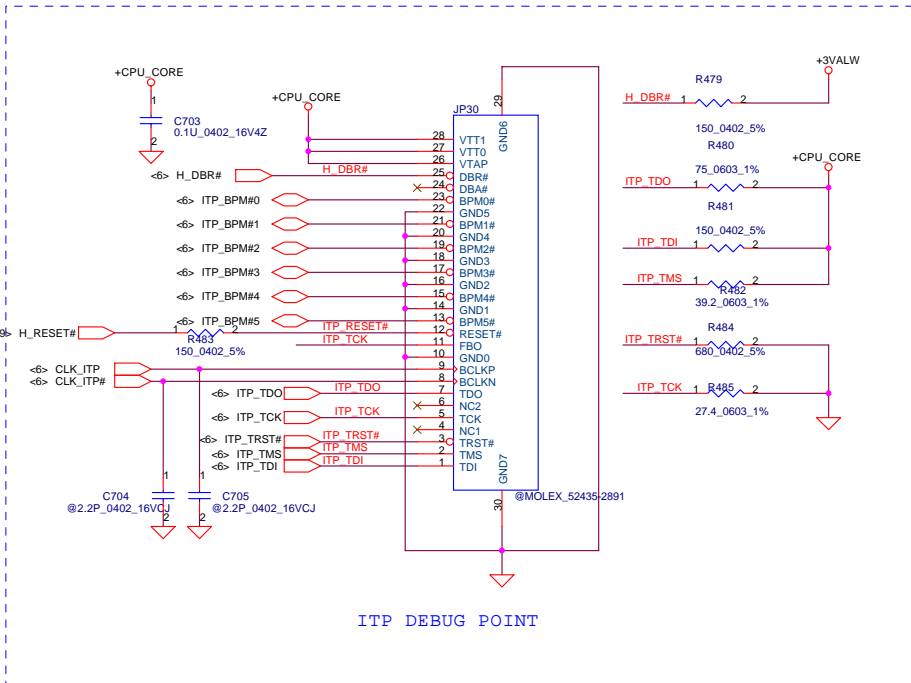
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File: CPU Decoupling CAP. & Fan control		
Size: Abacus-MTLA-1682	Document Number: Abacus-MTLA-1682	Rev: 0.2
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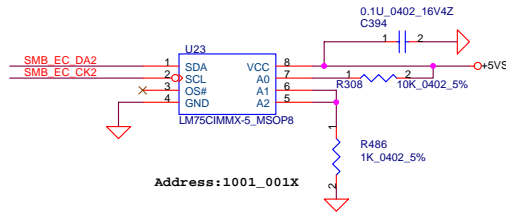
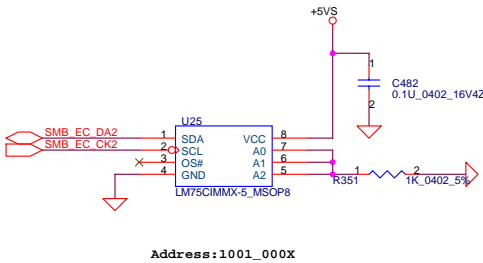


VID	4	3	2	1	0	V
	0	1	0	1	1	1.5750
	0	1	1	0	0	1.5500
	0	1	1	0	1	1.5250
	0	1	1	1	0	1.5000
	0	1	1	1	1	1.4750
	1	0	0	0	0	1.4500
	1	0	0	0	1	1.4250
	1	0	0	1	0	1.4000
	1	0	0	1	1	1.3750
	1	0	1	0	0	1.3500
	1	0	1	0	1	1.3250
	1	0	1	1	0	1.3000
	1	0	1	1	1	1.2750
	1	1	0	0	0	1.2500
	1	1	0	0	1	1.2250
	1	1	0	1	0	1.2000
	1	1	0	1	1	1.1750
	1	1	1	0	0	1.1500
	1	1	1	0	1	1.1250
	1	1	1	1	0	1.1000
	1	1	1	1	1	off



**ITP Debug Connector**

<6,32> SMB\_EC\_DA2  
<6,32> SMB\_EC\_CK2



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**CPU VID & ITP PORT**

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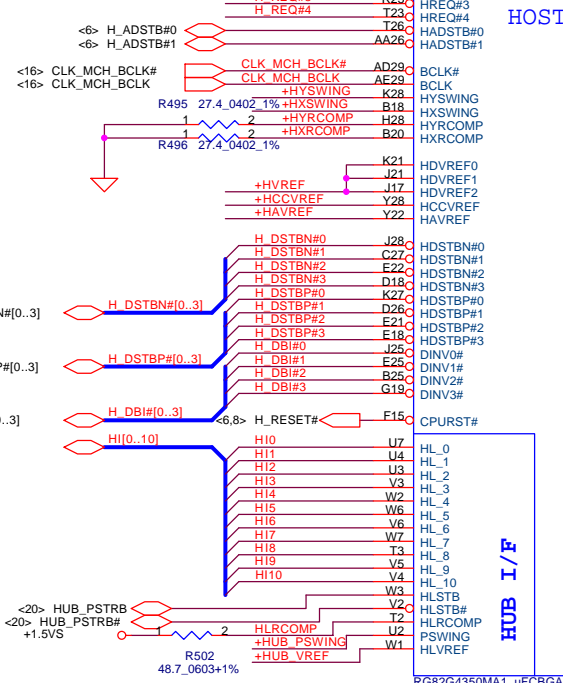
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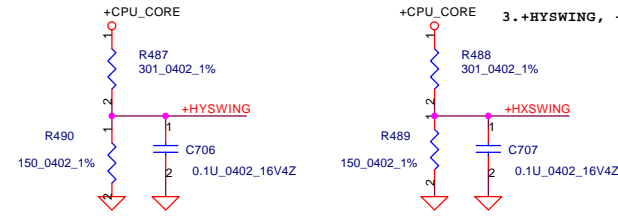


**Montara-GT**

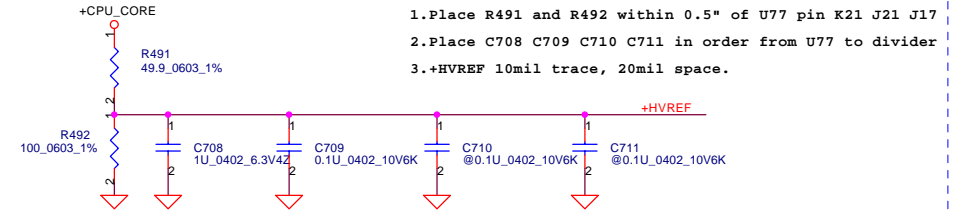
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HA#4	T25	HA#4	HD#1	H27	HD#1
HA#5	T28	HA#5	HD#2	K25	HD#2
HA#6	R27	HA#6	HD#3	L24	HD#3
HA#7	U23	HA#7	HD#4	J27	HD#4
HA#8	R24	HA#8	HD#5	G28	HD#5
HA#9	R24	HA#9	HD#6	L27	HD#6
HA#10	U28	HA#9	HD#6	L23	HD#7
HA#11	V28	HA#10	HD#7	L25	HD#8
HA#12	U27	HA#11	HD#8	J24	HD#9
HA#13	T27	HA#12	HD#9	H25	HD#10
HA#14	V27	HA#13	HD#10	K23	HD#11
HA#15	U26	HA#14	HD#11	G27	HD#12
HA#16	V26	HA#15	HD#12	K28	HD#13
HA#17	Y24	HA#16	HD#13	J23	HD#14
HA#18	V24	HA#17	HD#14	H26	HD#15
HA#19	V23	HA#18	HD#15	E25	HD#16
HA#20	W25	HA#19	HD#16	F26	HD#17
HA#21	Y25	HA#20	HD#17	B27	HD#18
HA#22	AA27	HA#21	HD#18	A23	HD#19
HA#23	W24	HA#22	HD#19	E27	HD#20
HA#24	W23	HA#23	HD#20	G25	HD#21
HA#25	W27	HA#24	HD#21	F28	HD#22
HA#26	Y27	HA#25	HD#22	D27	HD#23
HA#27	AA28	HA#26	HD#23	G24	HD#24
HA#28	W28	HA#27	HD#24	G28	HD#25
HA#29	AB27	HA#28	HD#25	G28	HD#26
HA#30	Y26	HA#29	HD#26	G22	HD#27
HA#31	AB28	HA#30	HD#27	C26	HD#28
		HA#31	HD#28	E26	HD#29
			HD#29	E26	HD#30
			HD#30	G23	HD#31
			HD#31	B28	HD#32
			HD#32	B21	HD#33
			HD#33	C21	HD#34
			HD#34	C24	HD#35
			HD#35	C23	HD#36
			HD#36	D22	HD#37
			HD#37	C25	HD#38
			HD#38	E24	HD#39
			HD#39	B24	HD#40
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			HD#41	E23	HD#42
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			HD#46	C20	HD#47
			HD#47	G18	HD#48
			HD#48	E19	HD#49
			HD#49	E20	HD#50
			HD#50	G17	HD#51
			HD#51	D20	HD#52
			HD#52	E19	HD#53
			HD#53	C19	HD#54
			HD#54	C17	HD#55
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			HD#63	C18	HD#63



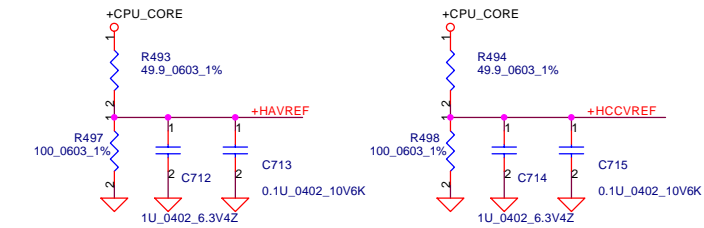
**HXSWING and HYSWING Ref. Voltage**



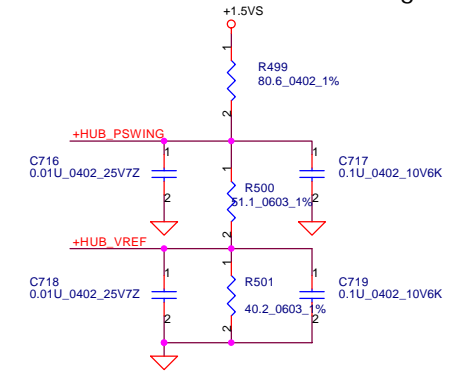
**Host data Ref. Voltage**



**Host Address Ref. Voltage**



**HUBLink reference Voltage**

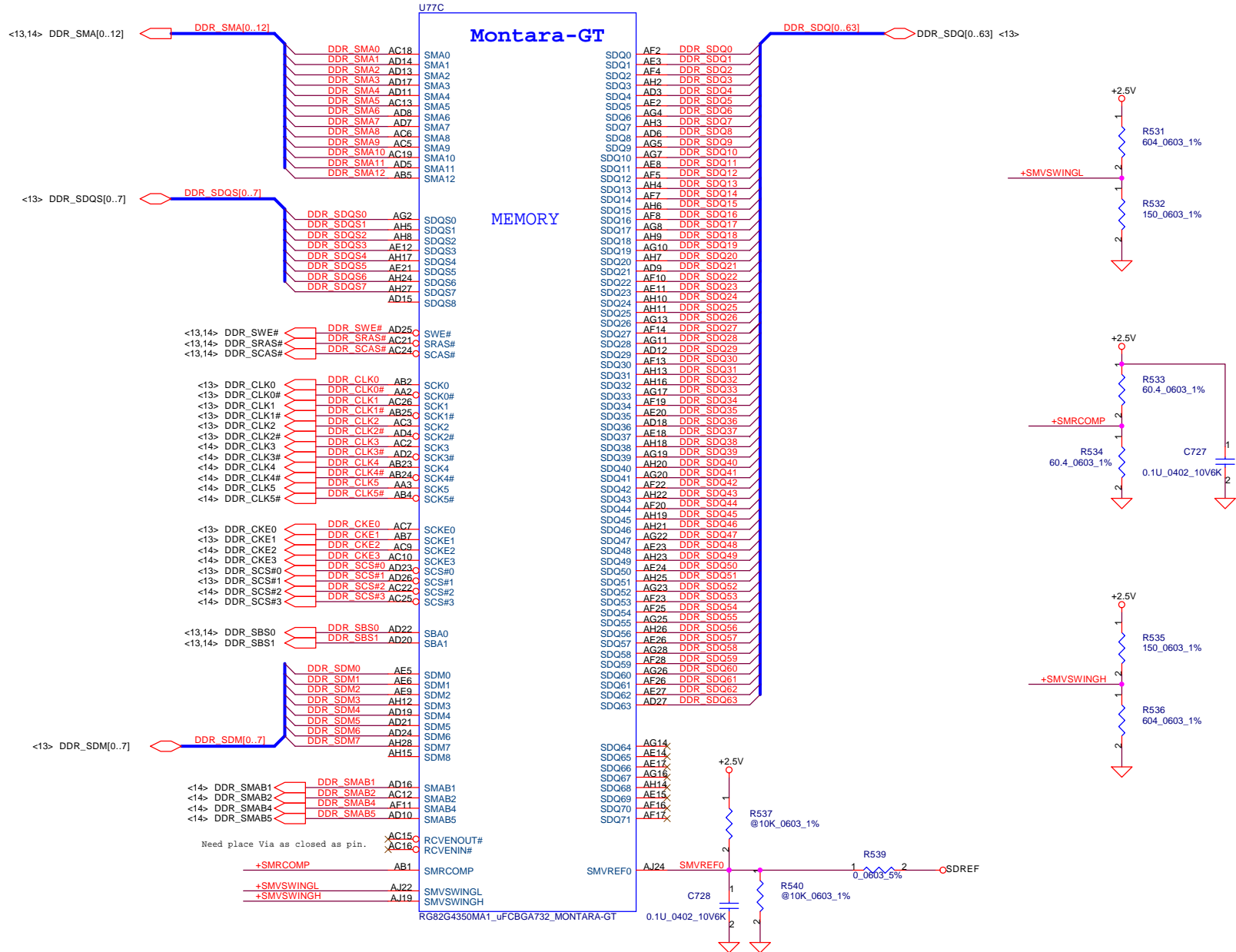


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Title		
Montara-GT (1/4)		
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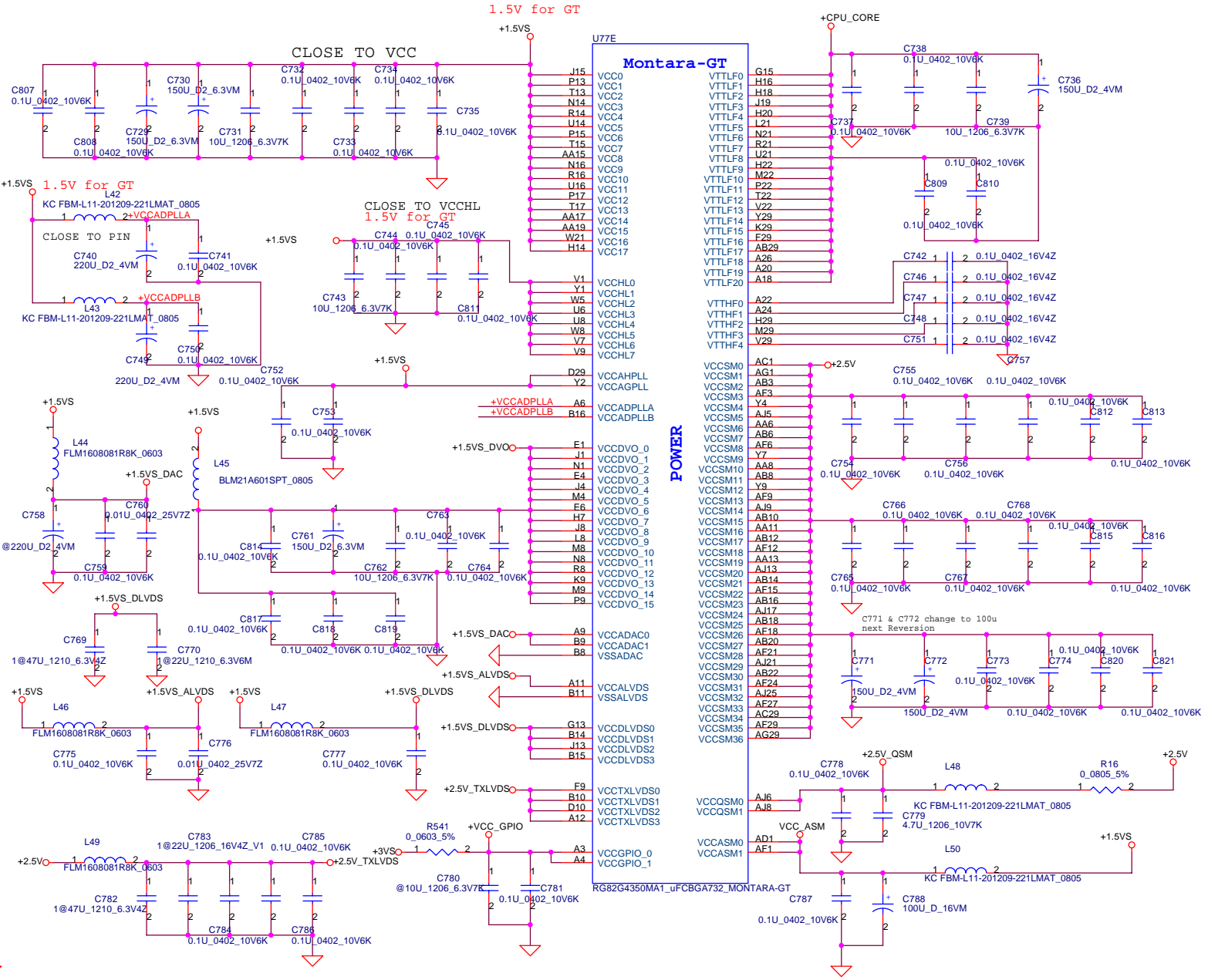
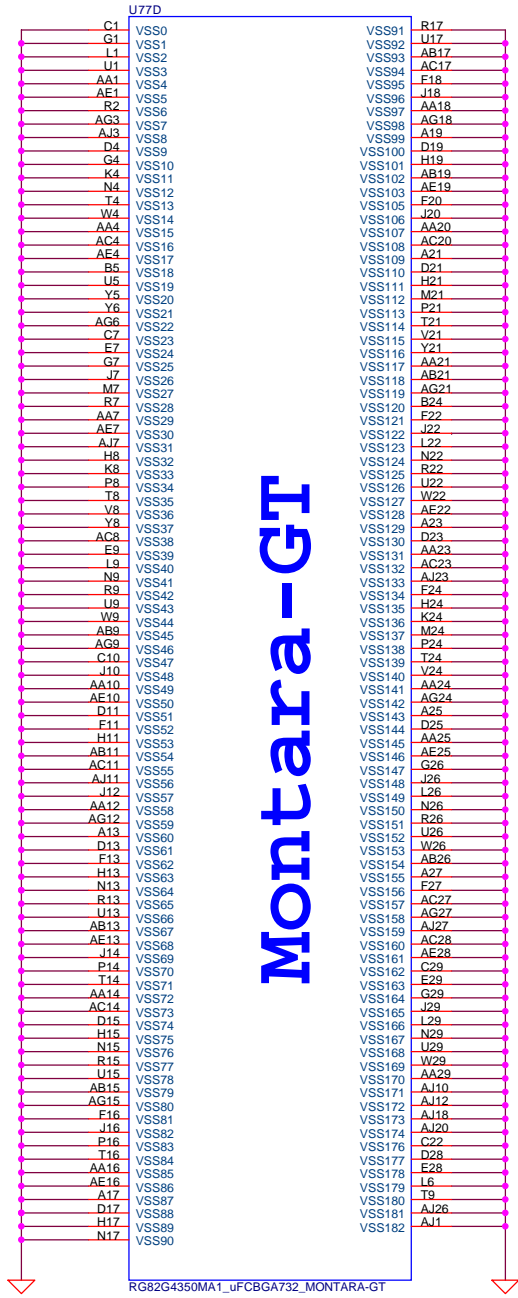
TOPOLOGY 2 FOR DDR  
 SMAA[12:6,3,0], SBA[1:0], SRAS#, SCAS#, SWE#

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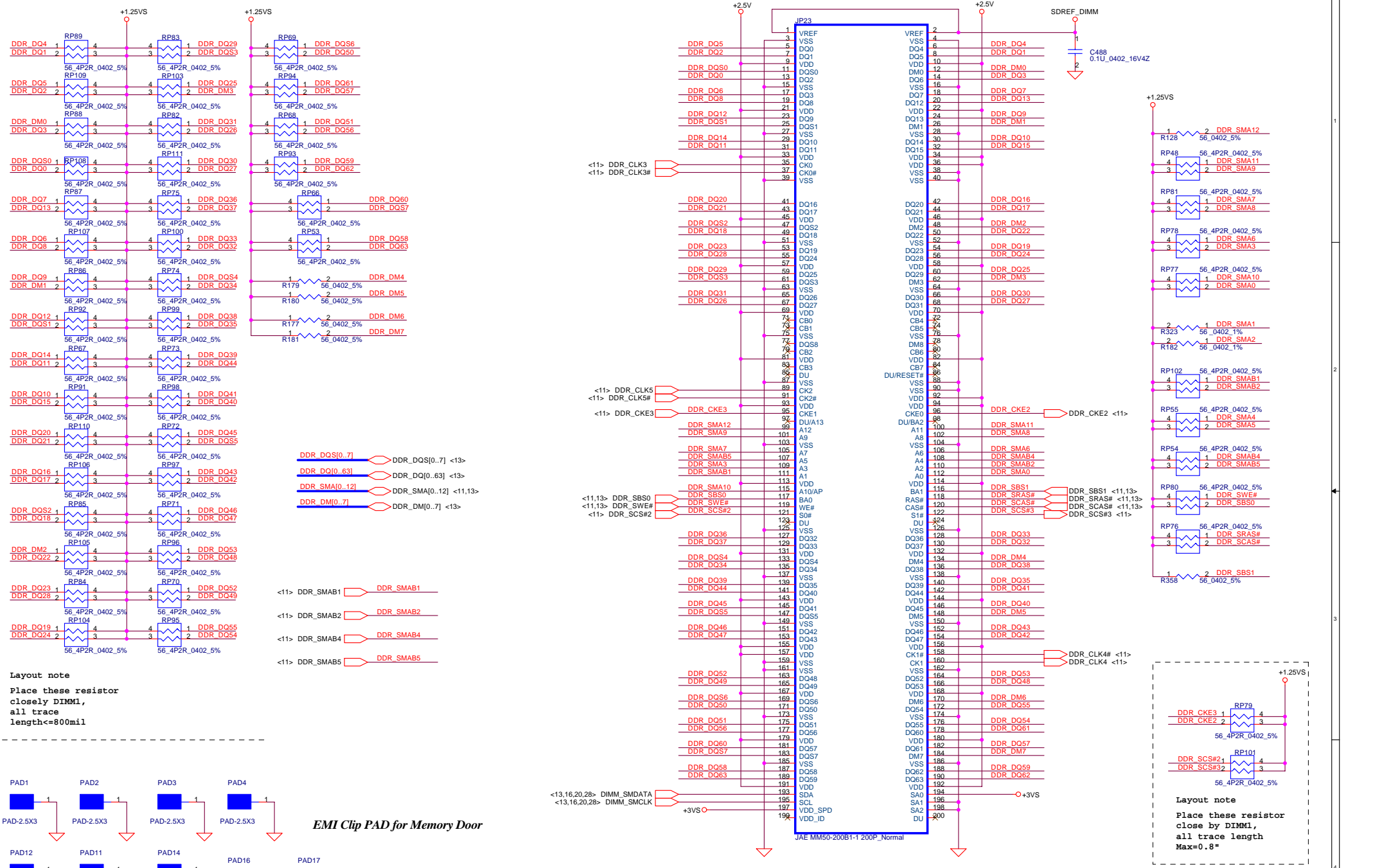
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Title Montara-GT (3/4)		
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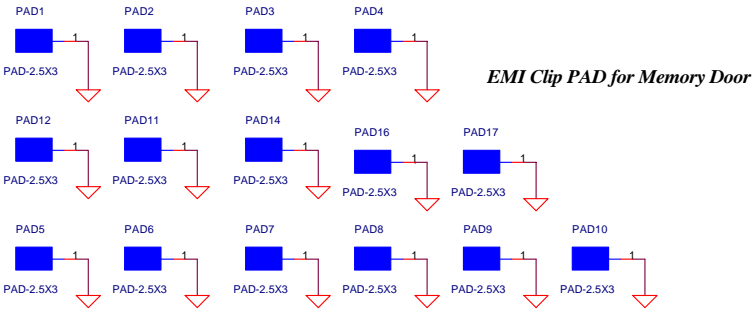
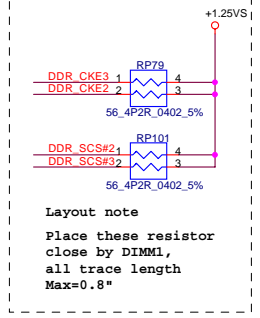
# Montara-GT







**Layout note**  
Place these resistor closely DIMM1, all trace length=<800mil



**DDR TOPOLOGY 2 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#**

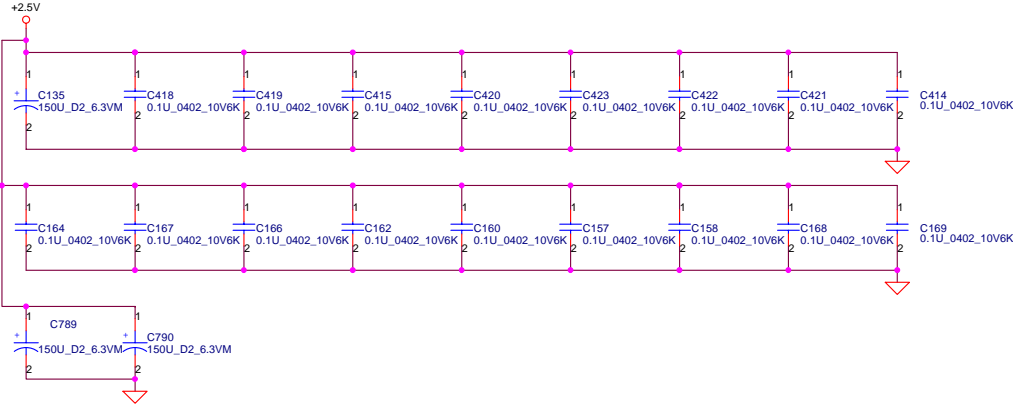
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Title		
DDR-SODIMM SLOT1		
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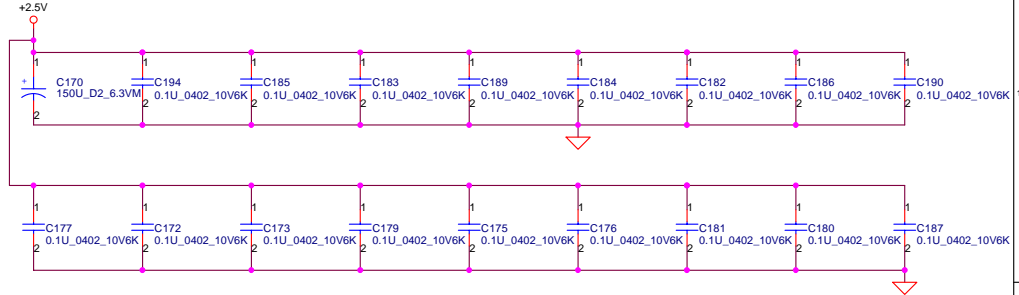
**Layout note :**

Distribute as close as possible to DDR-SODIMM0.



**Layout note :**

Distribute as close as possible to DDR-SODIMM1.



**Layout note :**

Place one cap close to every 2 pull up resistors termination to +1.25VS



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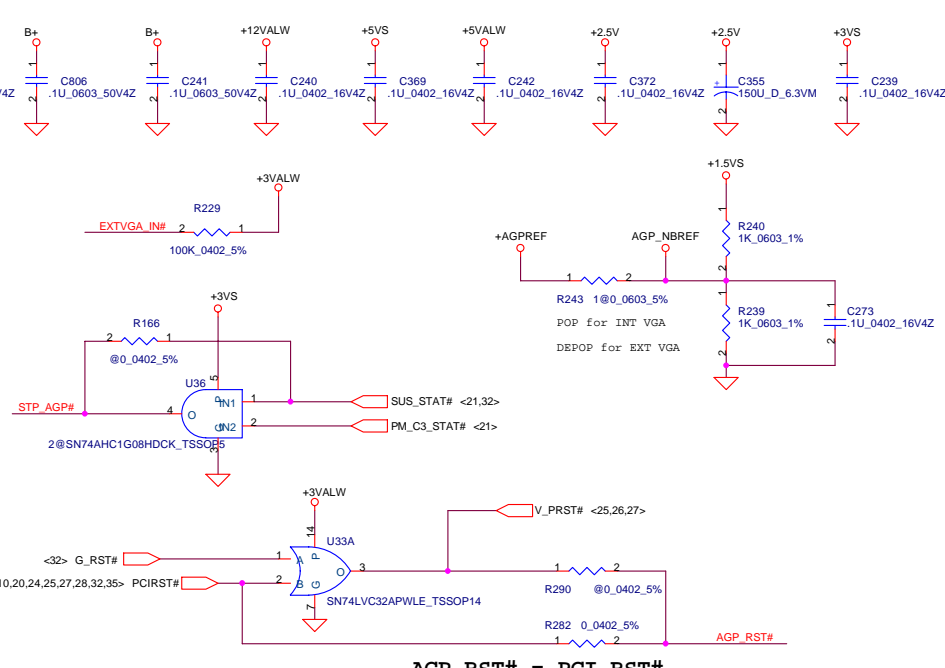
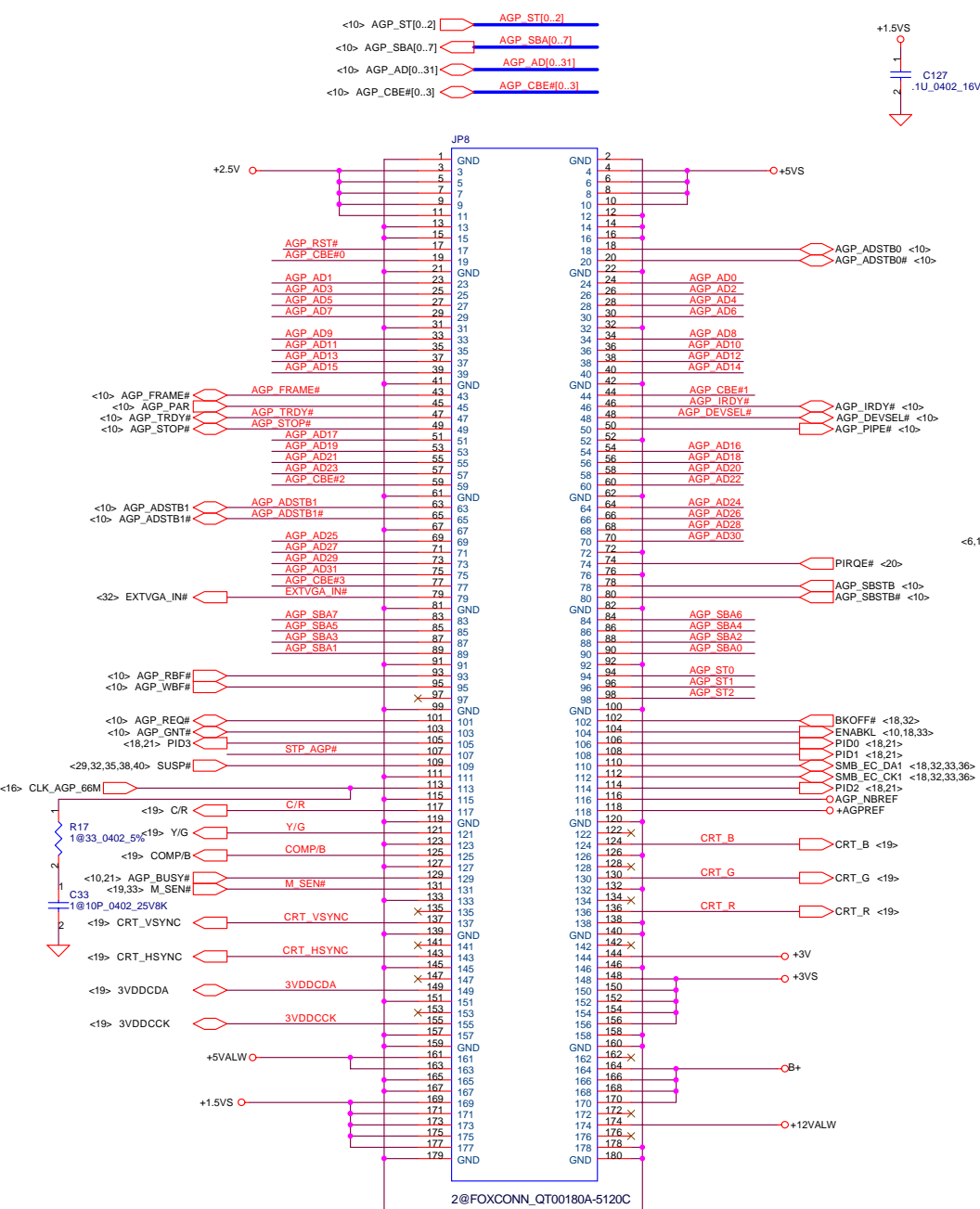
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Title		
DDR SODIMM Decoupling		
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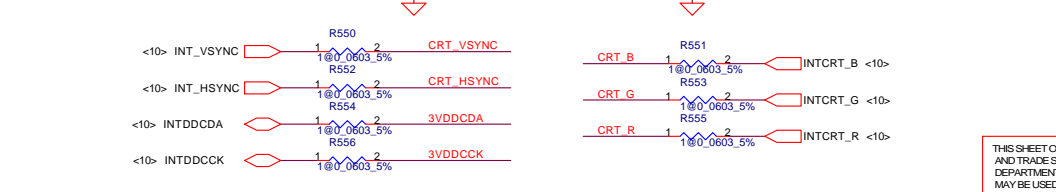
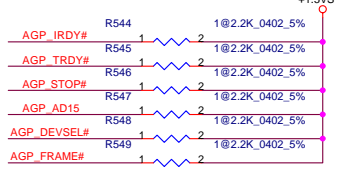






AGP\_RST# = PCI\_RST#

H: AGP L: DVO  
DVO Detect  
AGP\_PAR internal pull low



\* EXTVGA\_IN#  
1: internal graphic  
2: external AGP

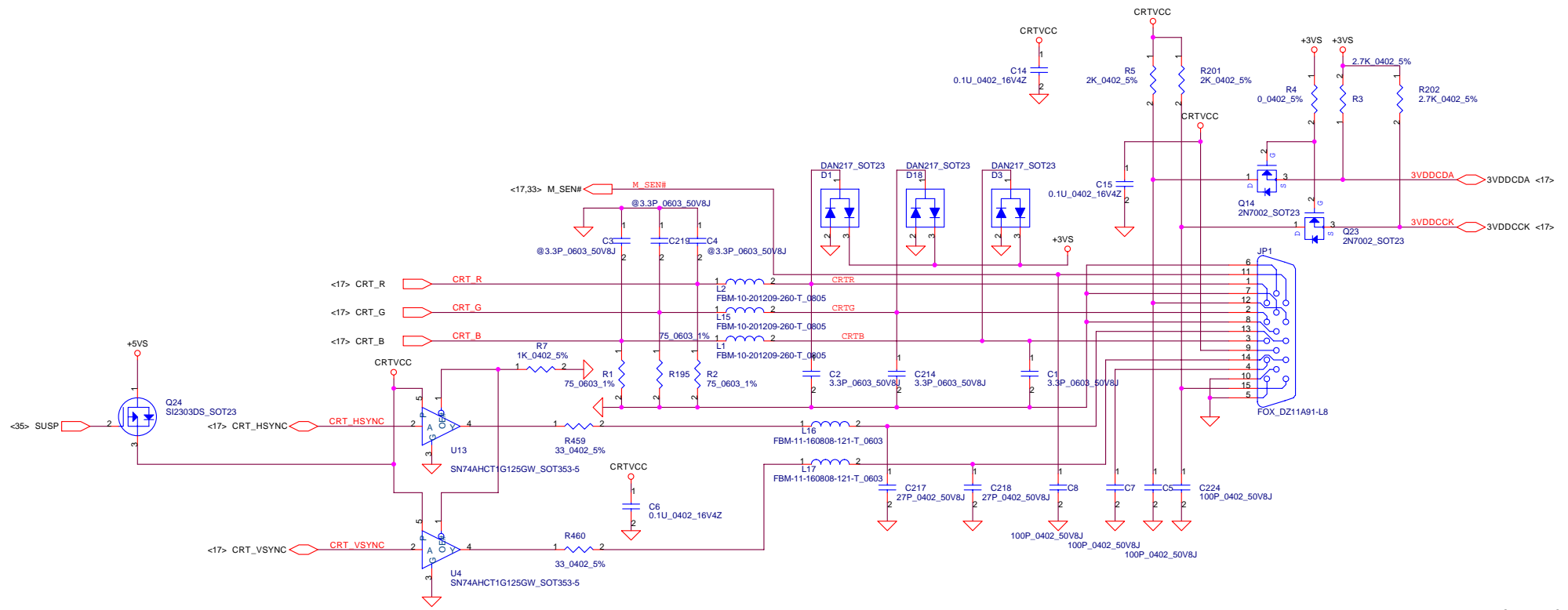
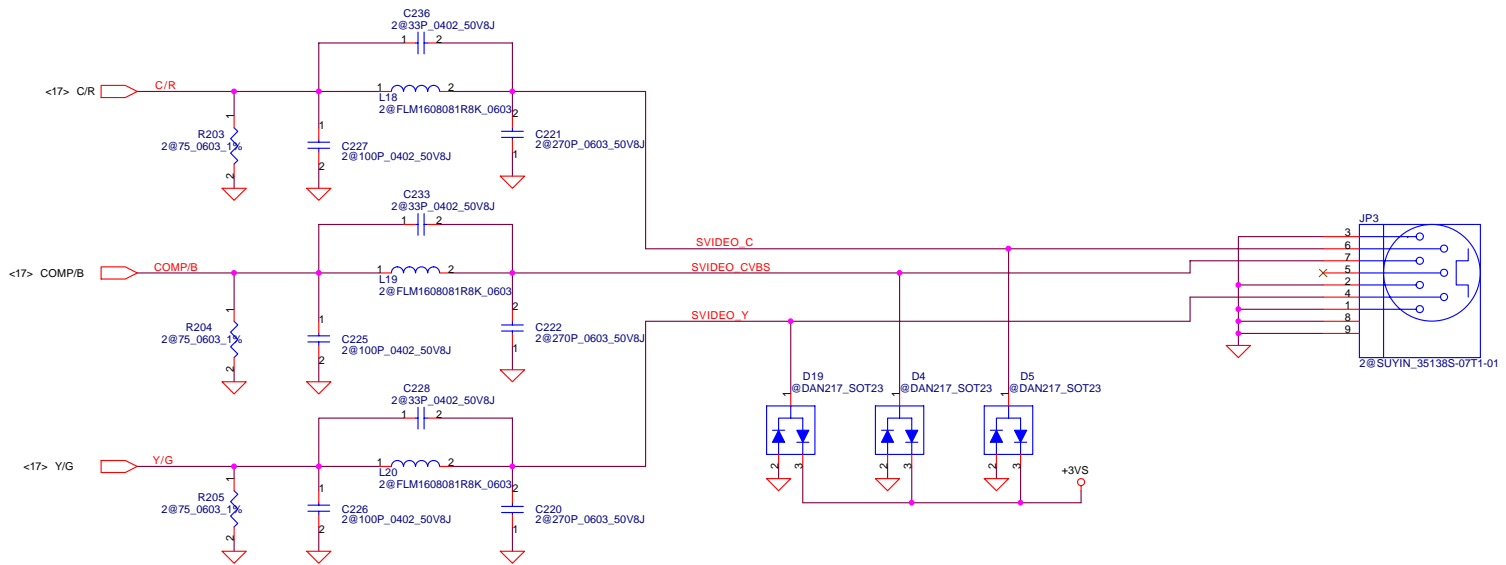
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External AGP

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TV OUT & CRT

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Title <b>TV OUT &amp; CRT</b>		
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U55C

# ICH4-M

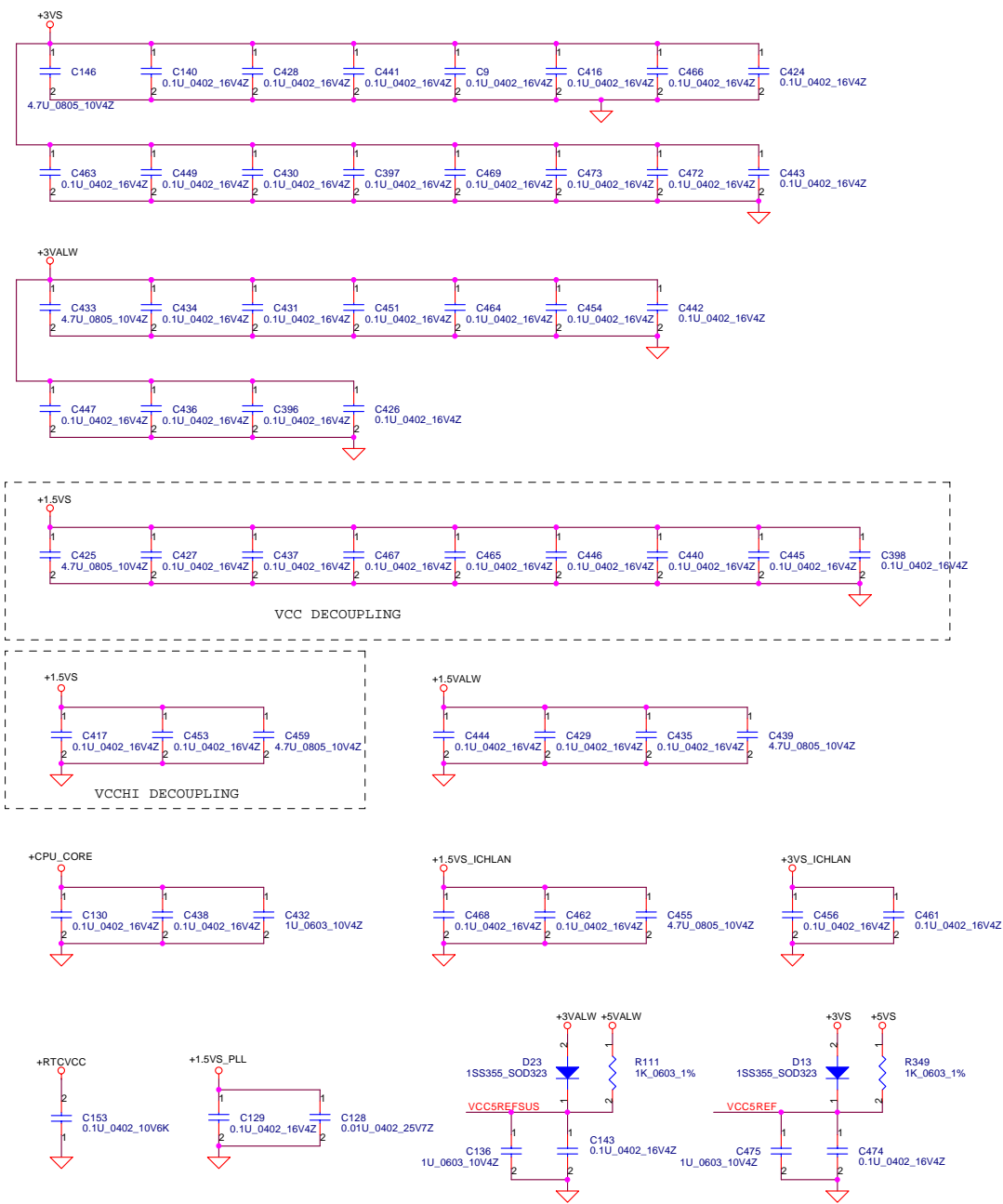
- D22 VSS0
- E10 VSS1
- E14 VSS2
- E16 VSS3
- E17 VSS4
- E18 VSS5
- E19 VSS6
- E21 VSS7
- E22 VSS8
- F8 VSS9
- G19 VSS10
- G21 VSS11
- G3 VSS12
- G6 VSS13
- H1 VSS14
- H6 VSS15
- K11 VSS16
- K13 VSS17
- K19 VSS18
- K23 VSS19
- K3 VSS20
- L10 VSS21
- L11 VSS22
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- Y19 VSS59
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- A16 VSS61
- A18 VSS62
- A20 VSS63
- A22 VSS64
- A4 VSS65
- AA12 VSS66
- AA16 VSS67
- AA22 VSS68
- AA3 VSS69
- AA9 VSS70
- AB20 VSS71
- AB7 VSS72
- AC1 VSS73
- AC10 VSS74
- AC14 VSS75
- AC18 VSS76
- AC23 VSS77
- AC5 VSS78
- B12 VSS79
- B16 VSS80
- B20 VSS81
- B18 VSS82
- B20 VSS83
- B22 VSS84
- B9 VSS85
- C15 VSS86
- C17 VSS87
- C19 VSS88
- C21 VSS89
- C23 VSS90
- D6 VSS91
- D1 VSS92
- D12 VSS93
- D15 VSS94
- D17 VSS95
- D19 VSS96
- D21 VSS97
- D23 VSS98
- D4 VSS99
- DB VSS100
- A1 VSS101

## GND POWER

- A5 VCC3.3\_0
- AC17 VCC3.3\_1
- B2 VCC3.3\_2
- B2 VCC3.3\_3
- H18 VCC3.3\_4
- H18 VCC3.3\_5
- J1 VCC3.3\_6
- J18 VCC3.3\_7
- K6 VCC3.3\_8
- M10 VCC3.3\_9
- P12 VCC3.3\_10
- P6 VCC3.3\_11
- U1 VCC3.3\_12
- V10 VCC3.3\_13
- V16 VCC3.3\_14
- V18 VCC3.3\_15
  
- E11 VCCSUS3.3\_0
- F10 VCCSUS3.3\_1
- F15 VCCSUS3.3\_2
- F16 VCCSUS3.3\_3
- F17 VCCSUS3.3\_4
- F18 VCCSUS3.3\_5
- K14 VCCSUS3.3\_6
- V7 VCCSUS3.3\_7
- V8 VCCSUS3.3\_8
- V9 VCCSUS3.3\_9
  
- K10 VCC1.5\_0
- K12 VCC1.5\_1
- K18 VCC1.5\_2
- K22 VCC1.5\_3
- P10 VCC1.5\_4
- T18 VCC1.5\_5
- U19 VCC1.5\_6
- V14 VCC1.5\_7
  
- E12 VCCSUS1.5\_0
- E13 VCCSUS1.5\_1
- E20 VCCSUS1.5\_2
- F14 VCCSUS1.5\_3
- G18 VCCSUS1.5\_4
- R6 VCCSUS1.5\_5
- T6 VCCSUS1.5\_6
- U6 VCCSUS1.5\_7
  
- E7 VCC5REF1
- V6 VCC5REF2
  
- F15 VCC5REFSUS1
  
- L23 VCCHI\_0
- M14 VCCHI\_1
- P18 VCCHI\_2
- T22 VCCHI\_3
  
- AA23 VCC\_CPU\_IO\_0
- P14 VCC\_CPU\_IO\_1
- U18 VCC\_CPU\_IO\_2
  
- C22 VCCPLL
- R85 R85 0.0805\_3% 1.5VS
  
- AB5 VCCRTC
  
- E9 VCCLAN3.3\_0
- F9 VCCLAN3.3\_1
- R338 R338 0.0805\_3% 3VS
  
- F6 VCCLAN1.5\_0
- F7 VCCLAN1.5\_1
- R332 R332 0.0805\_3% 1.5VS

FW92801DBM\_BGA421

# ICH4-M



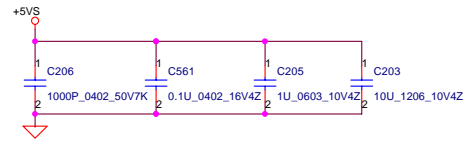
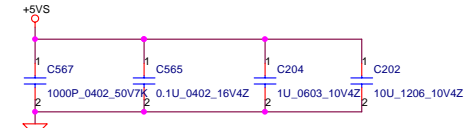
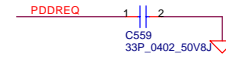
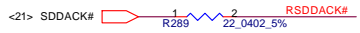
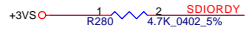
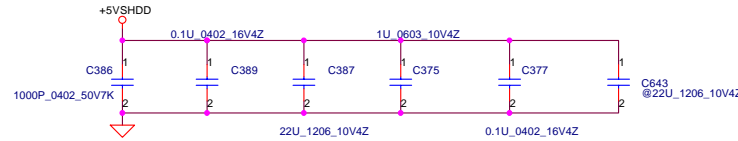
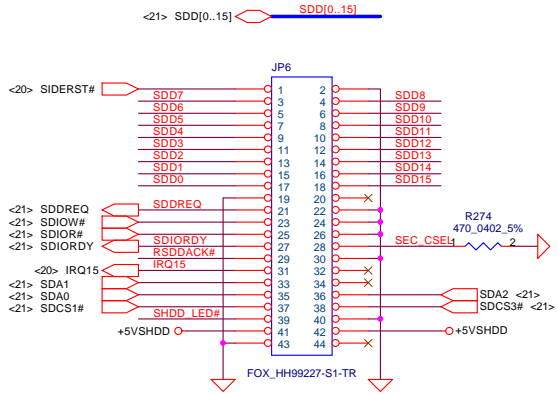
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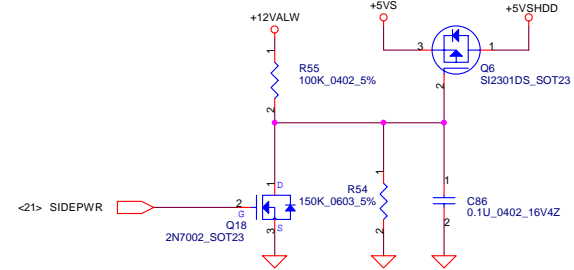
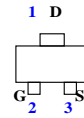
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INTEL ICH4 (33)		
Size	Document Number	Rev
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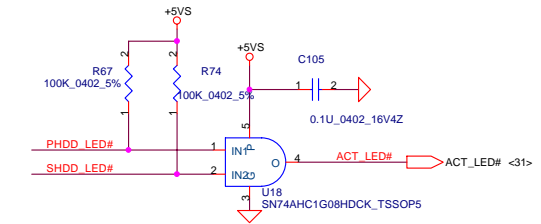
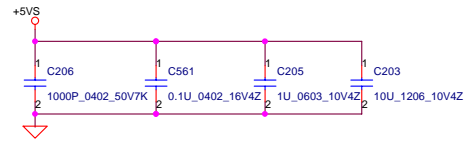
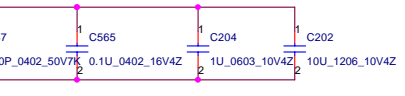
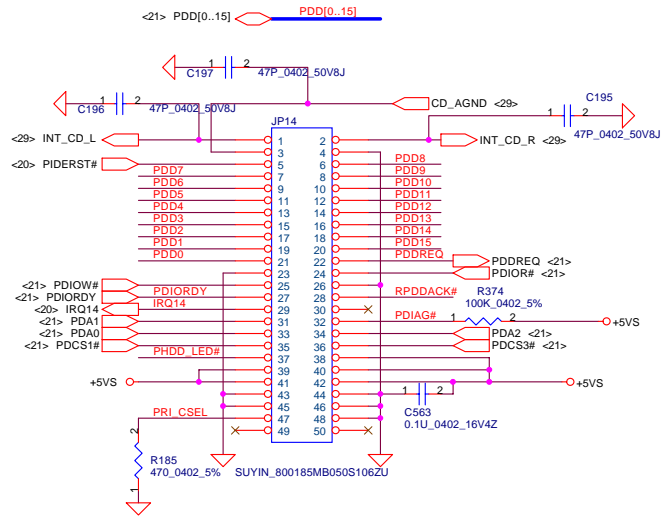
**HDD Connector**



SI2301DS: P CHANNEL  
 VGS: -4.5V, RDS: 130 mOHM  
 VGS: -2.5V, RDS: 190mOHM  
 Id(MAX): 2.3A  
 VGS(MAX): +-8V



**CD-ROM Connector**

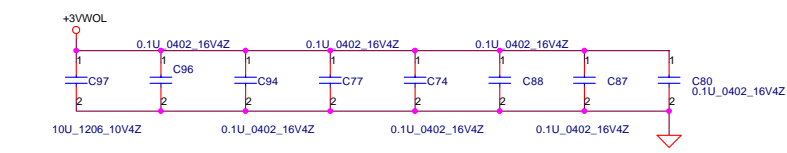


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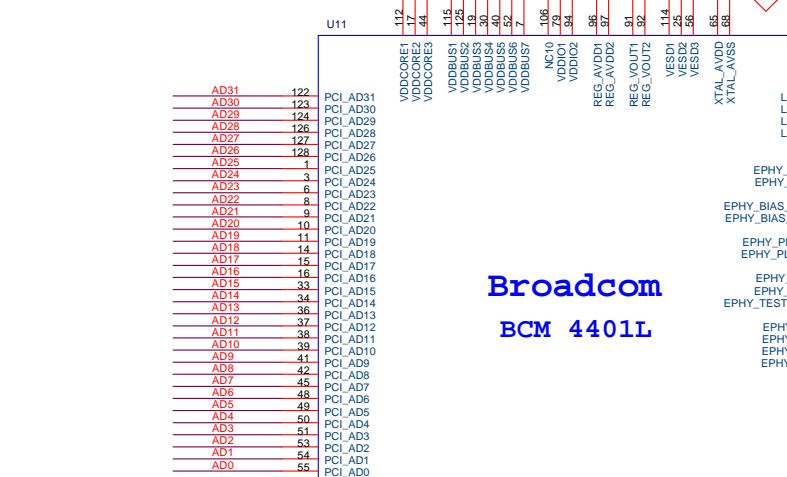
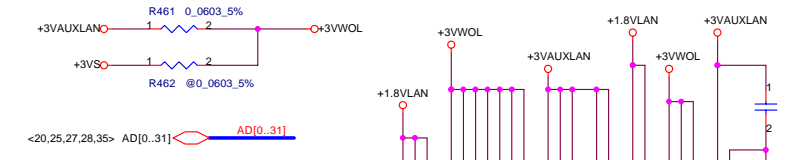
**Compal Electronics, Inc.**

Title		
IDE/FDD/CD-ROM Module		
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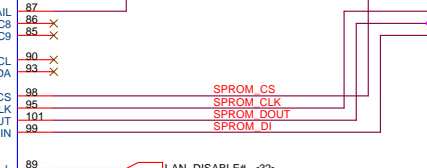
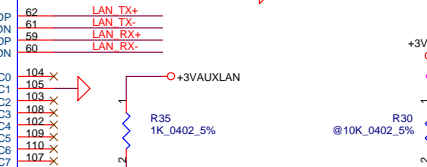
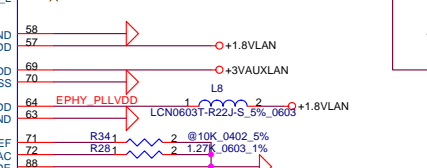
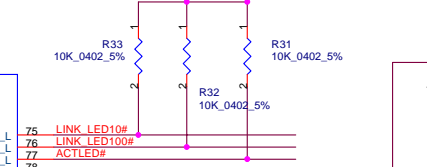
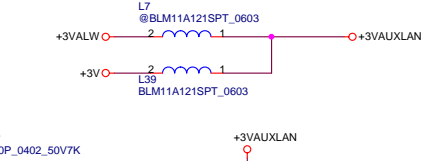
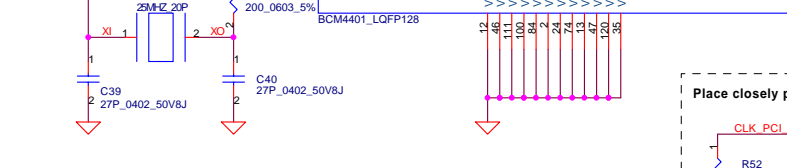
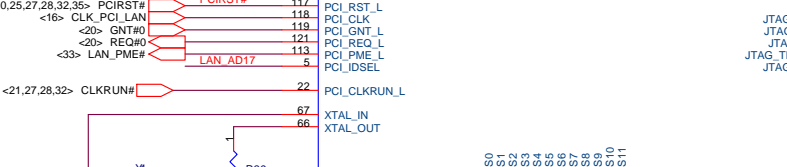
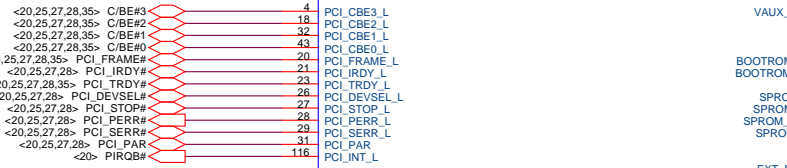
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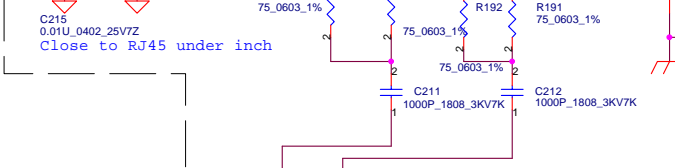
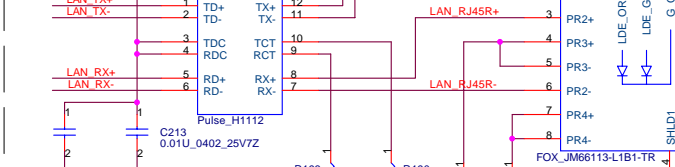
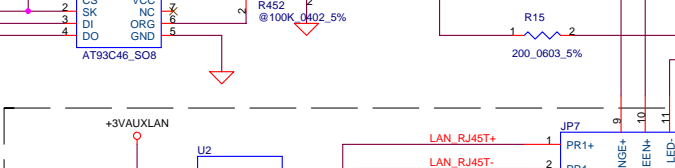
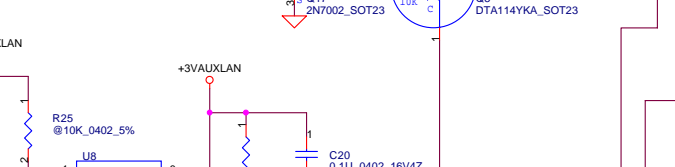
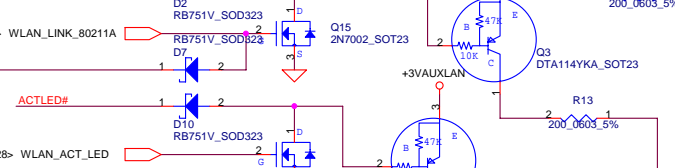
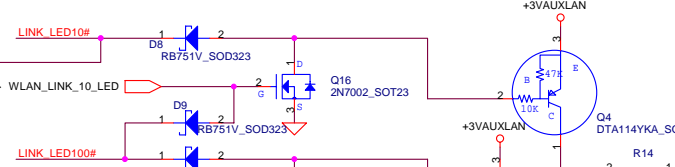
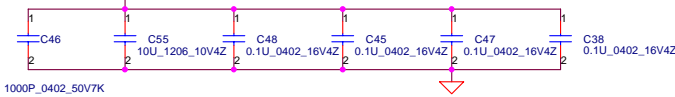
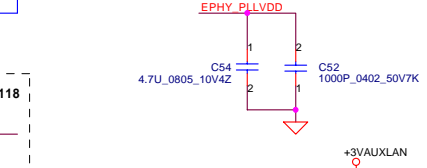
WLAN	LOM	LED (JP28)
WLAN_LINK_80211A	LINK_LED100#	ORANGE (100M)
WLAN_LINK_10_LDE	LINK_LED10#	GREEN (10M)
WLAN_ACT_LED	ACTLED#	YELLOW
WLAN_LINK_80211A	NC	ORANGE/GREEN
WLAN_LINK_10_LDE		



**Broadcom  
BCM 4401L**



	SPROM_DOUT	SPROM_CLK
1Kb	None	None
4Kb	10K Pullup	None
16Kb	None	10K Pullup



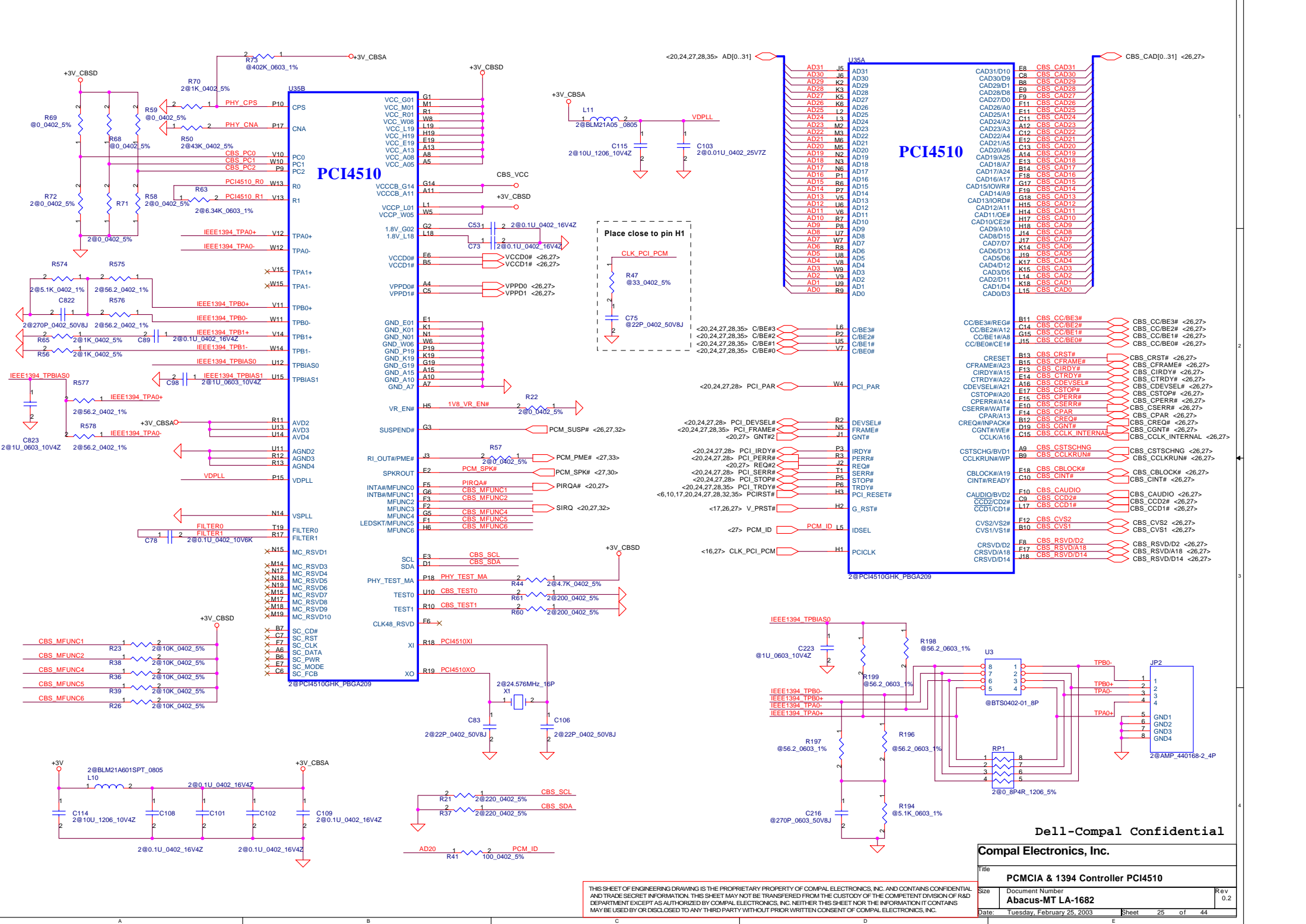
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**Compal Electronics, Inc.**  
**BROADCOM 4401L LAN**

Title	BROADCOM 4401L LAN	
Size	Document Number	Rev
	Abacus-MT LA-1682	0.2
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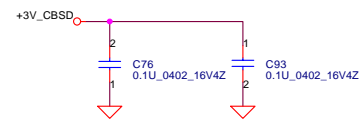
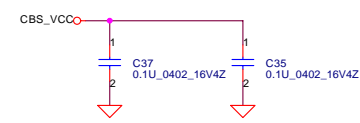
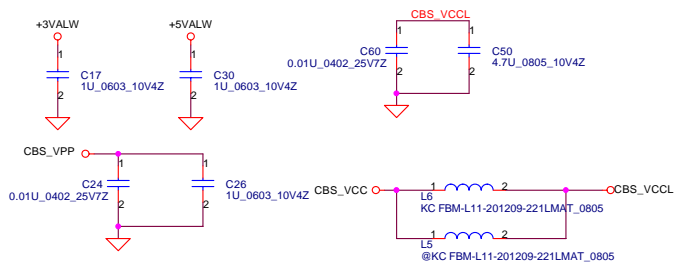
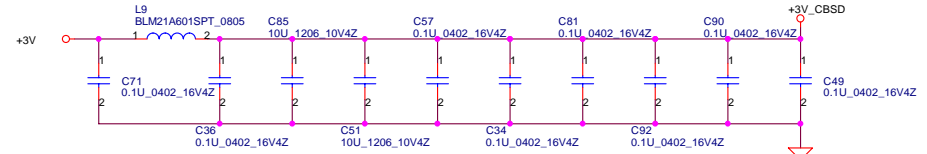
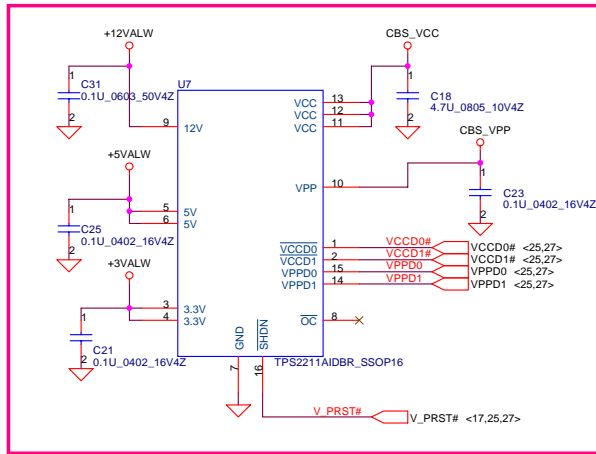
Title: PCMCIA & 1394 Controller PCI4510

Size: Document Number: Abacus-MT LA-1682

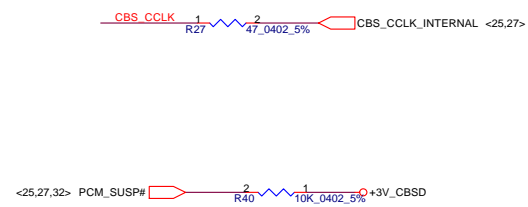
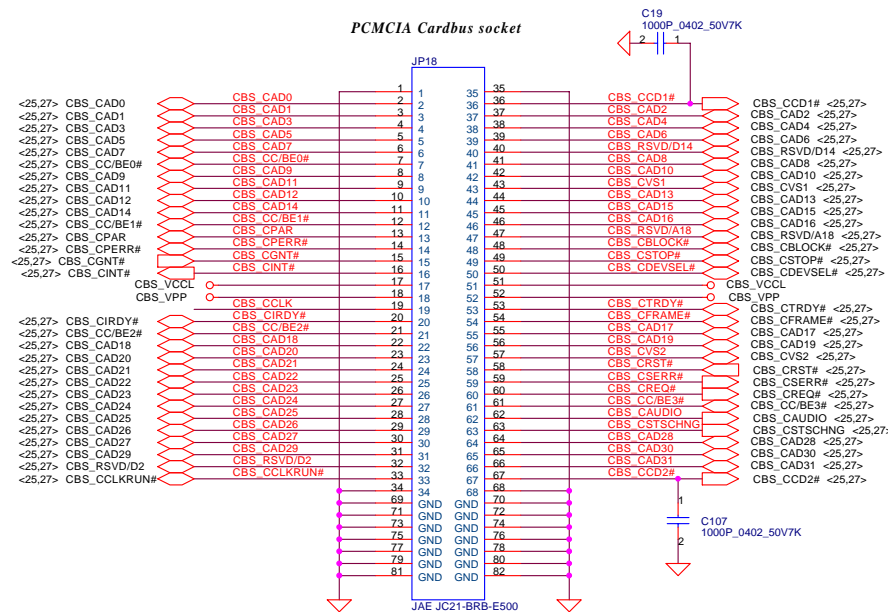
Date: Tuesday, February 25, 2003 Sheet 25 of 44 Rev 0.2

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PCMCIA Power Controller



PCMCIA Cardbus socket



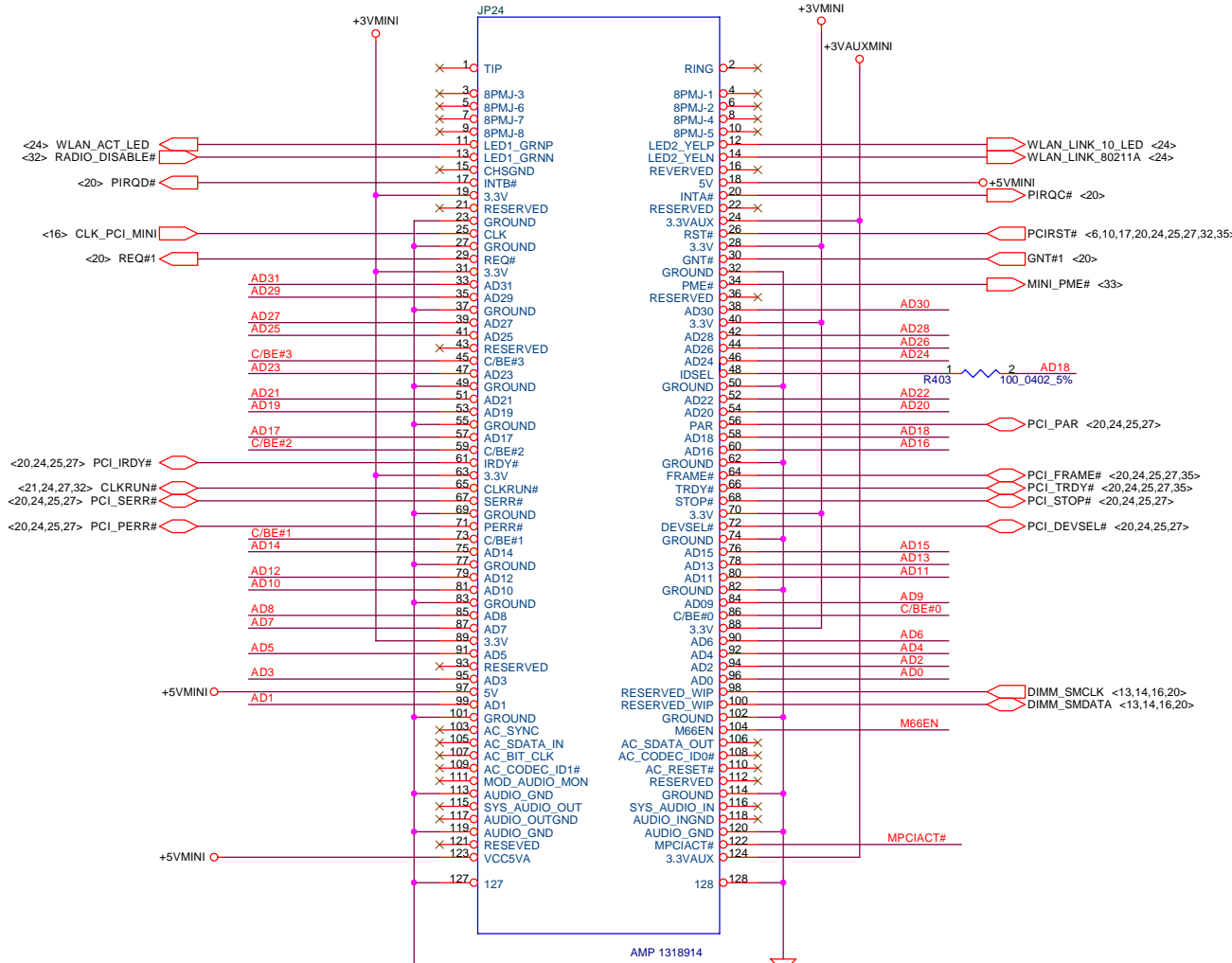
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Title <b>PCMCIA Socket</b>		
Size	Document Number <b>Abacus-MT LA-1682</b>	Rev 0.2
Date	Tuesday, February 25, 2003	Sheet 26 of 44

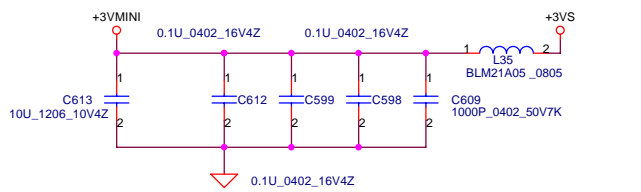
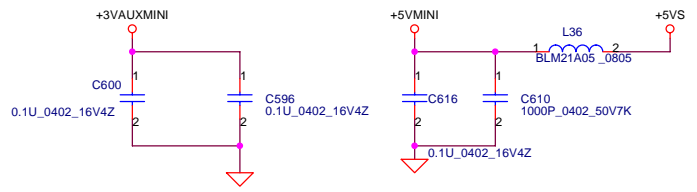
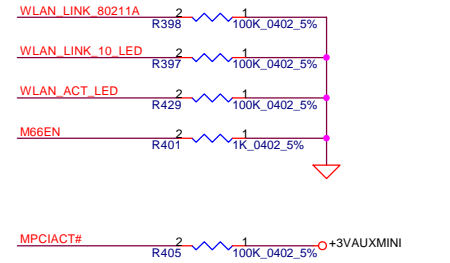
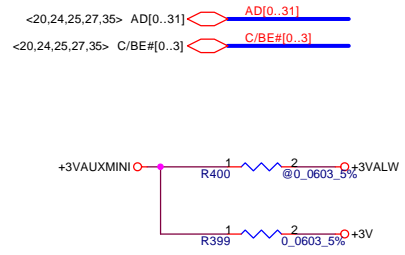
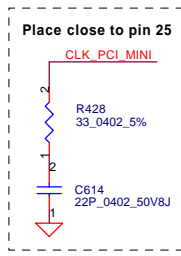
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# MINI PCI TYPE III



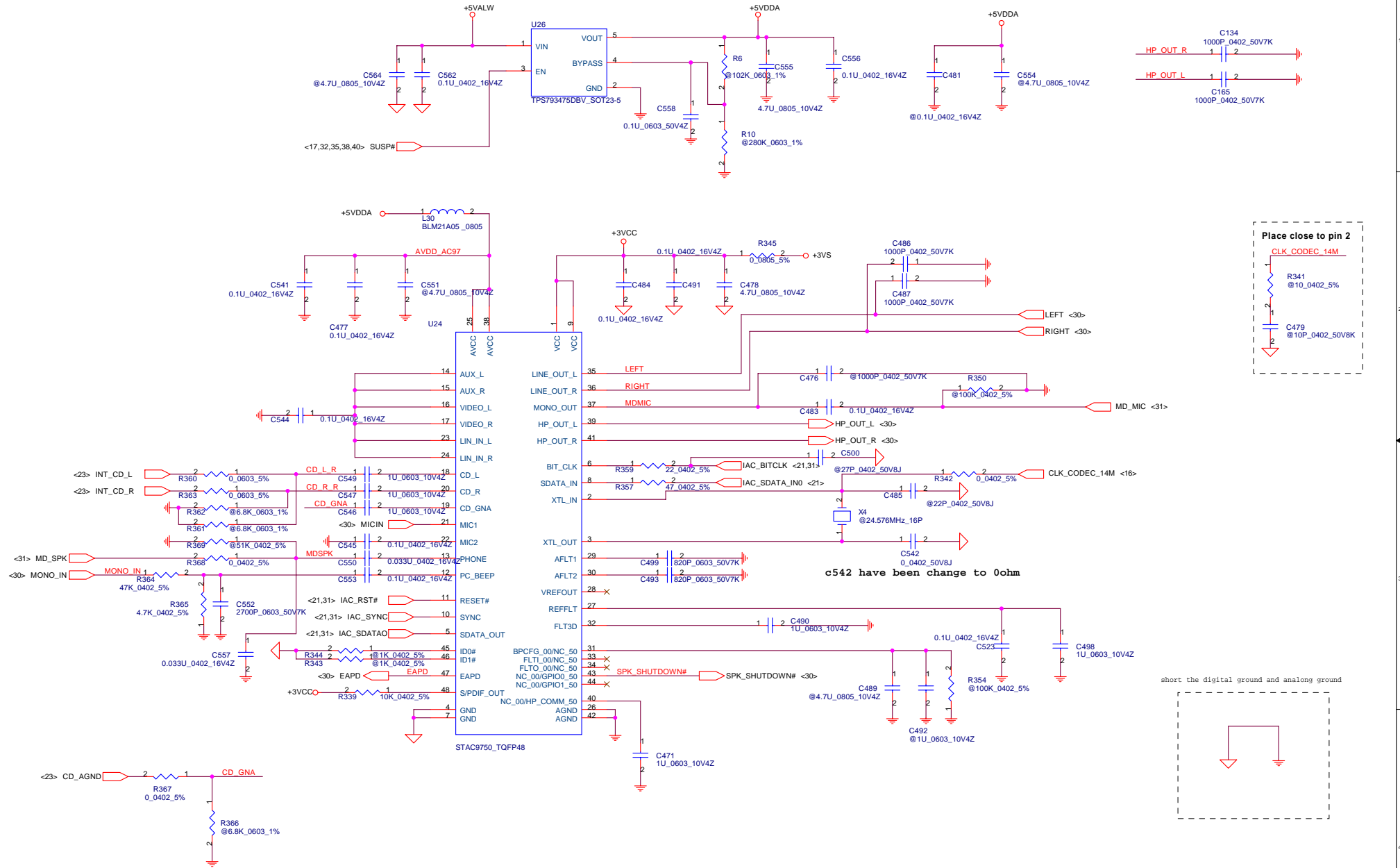
WIRELESS SUPPORT ONLY



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Compal Electronics, Inc.		
Title: MiniPci Port		
Size	Document Number: Abacus-MT LA-1682	Rev: 0.2
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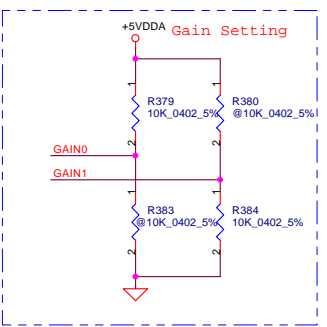
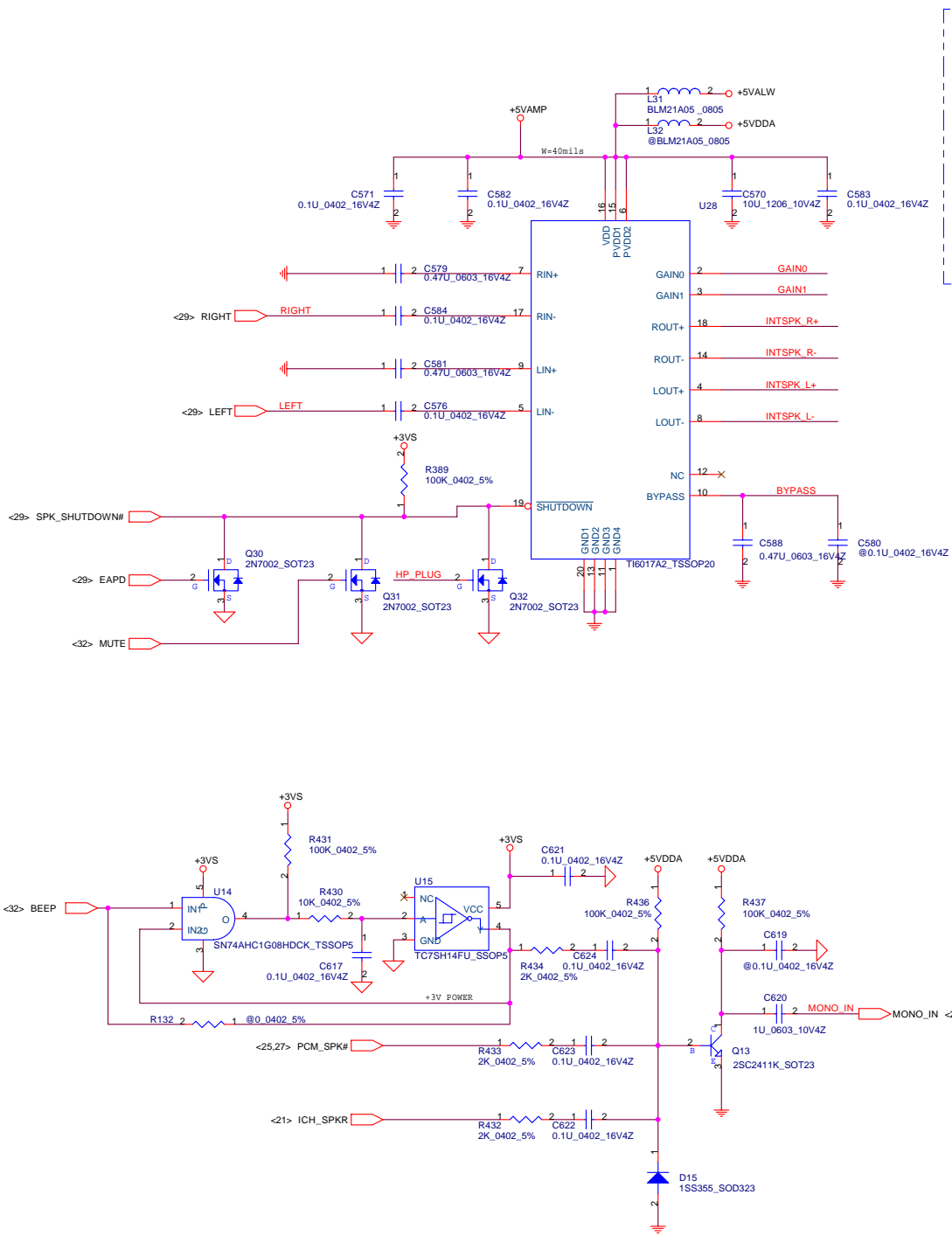


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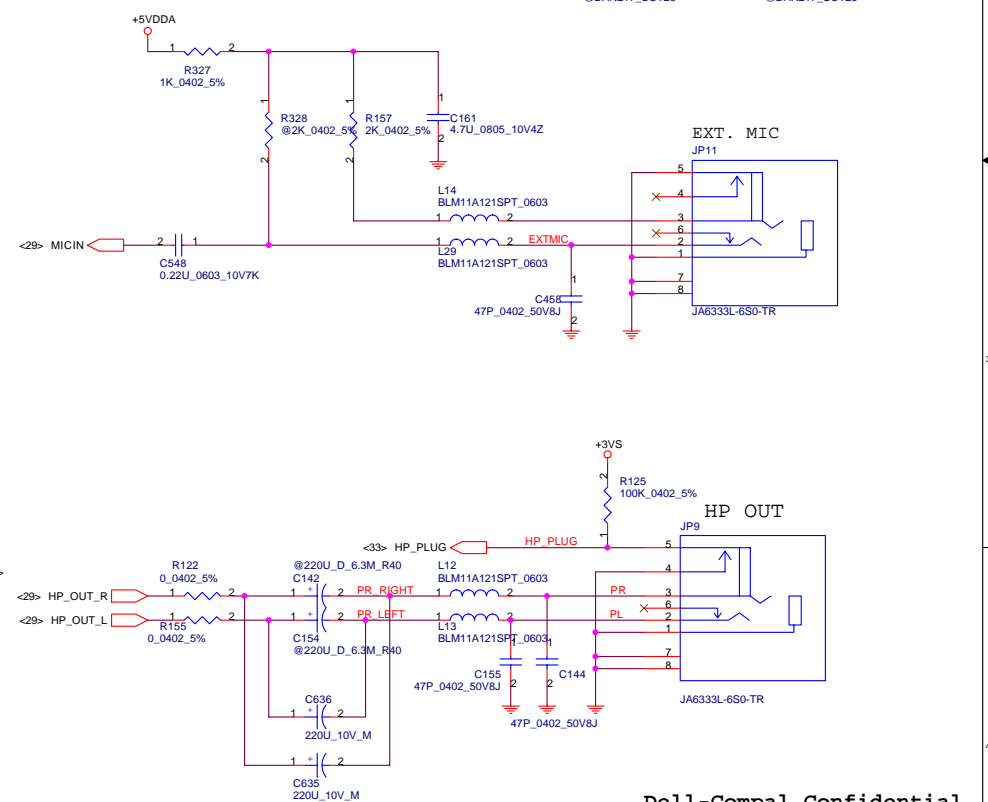
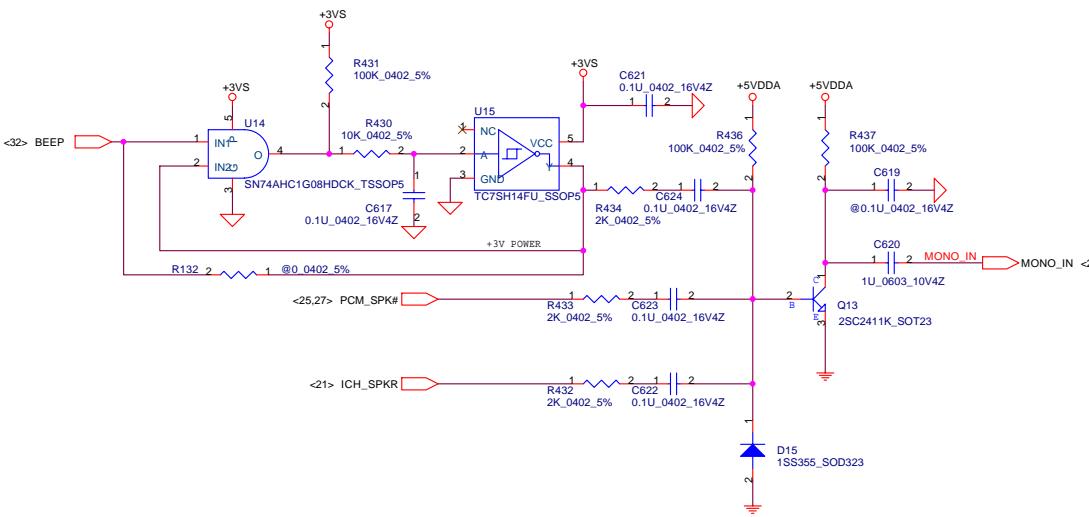
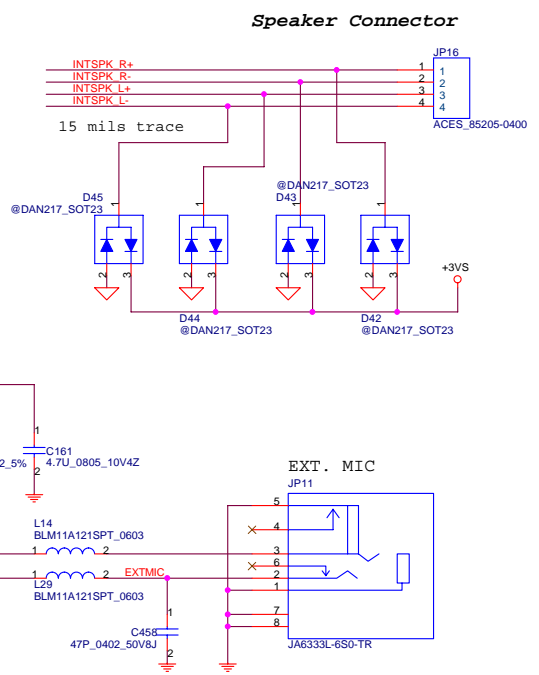
Compal Electronics, Inc.

Title		
AC97 CODEC		
Size	Document Number	Rev
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GAIN0	GAIN1	AV (inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm



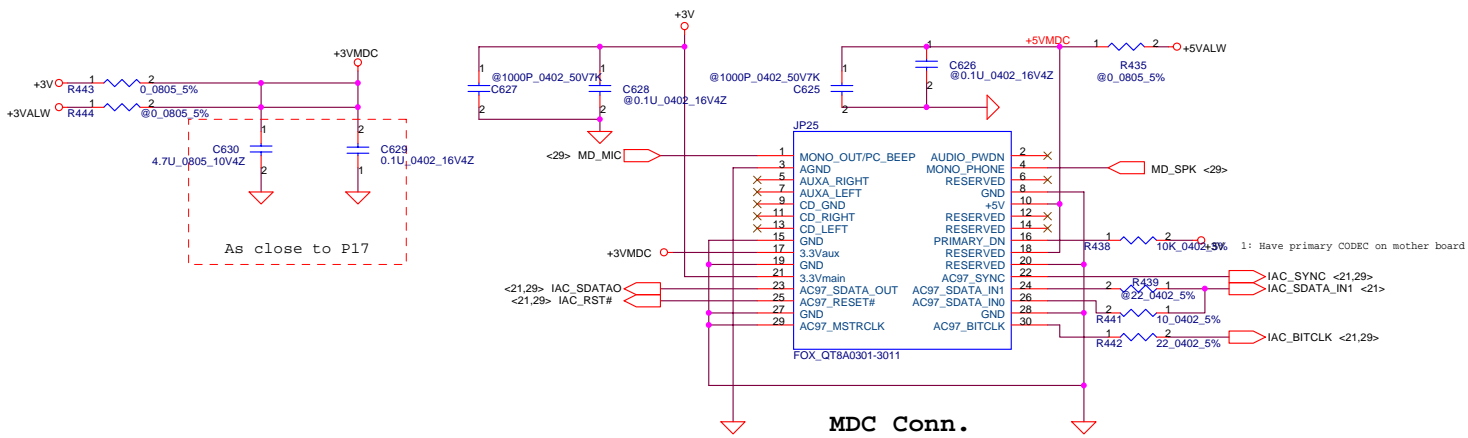
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AMP & Audio Jack

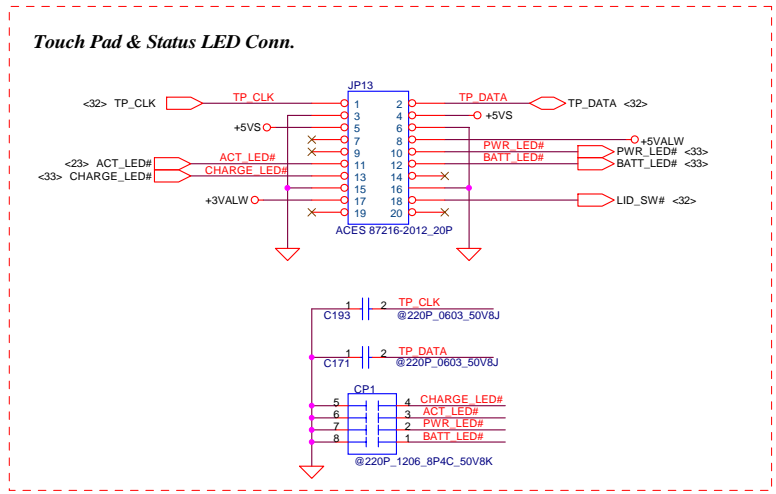
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Size	Document Number	Rev
	Abacus-MT LA-1682	0.2
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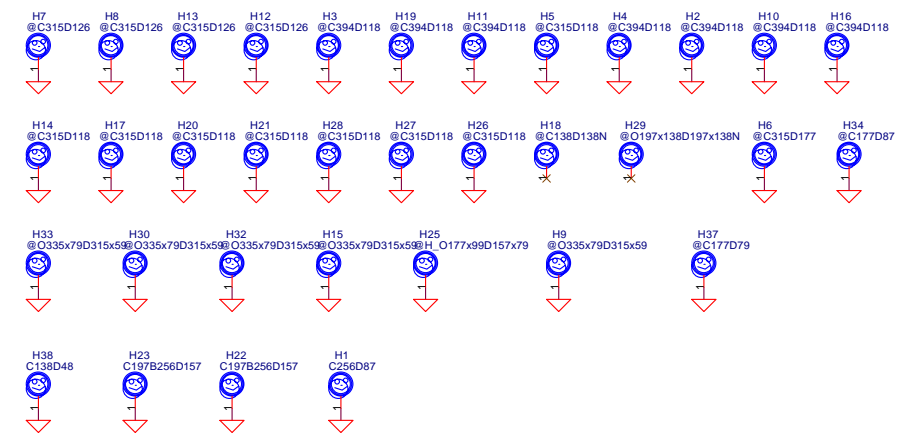


**MDC Conn.**

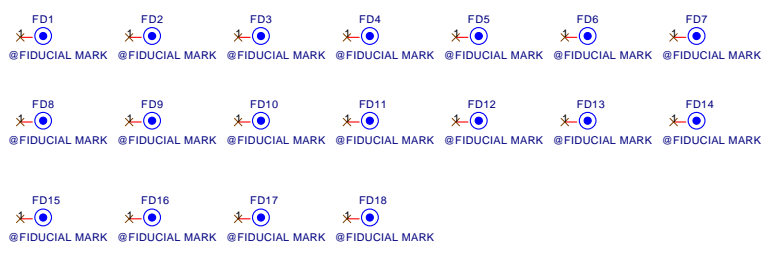
**MDC Note**  
 Pin 1 is NC for Pctel and connexant MDC modem  
 Pin 2 is NC for Pctel and connexant MDC modem



**Screw Hole**



**Fiducial Mark**

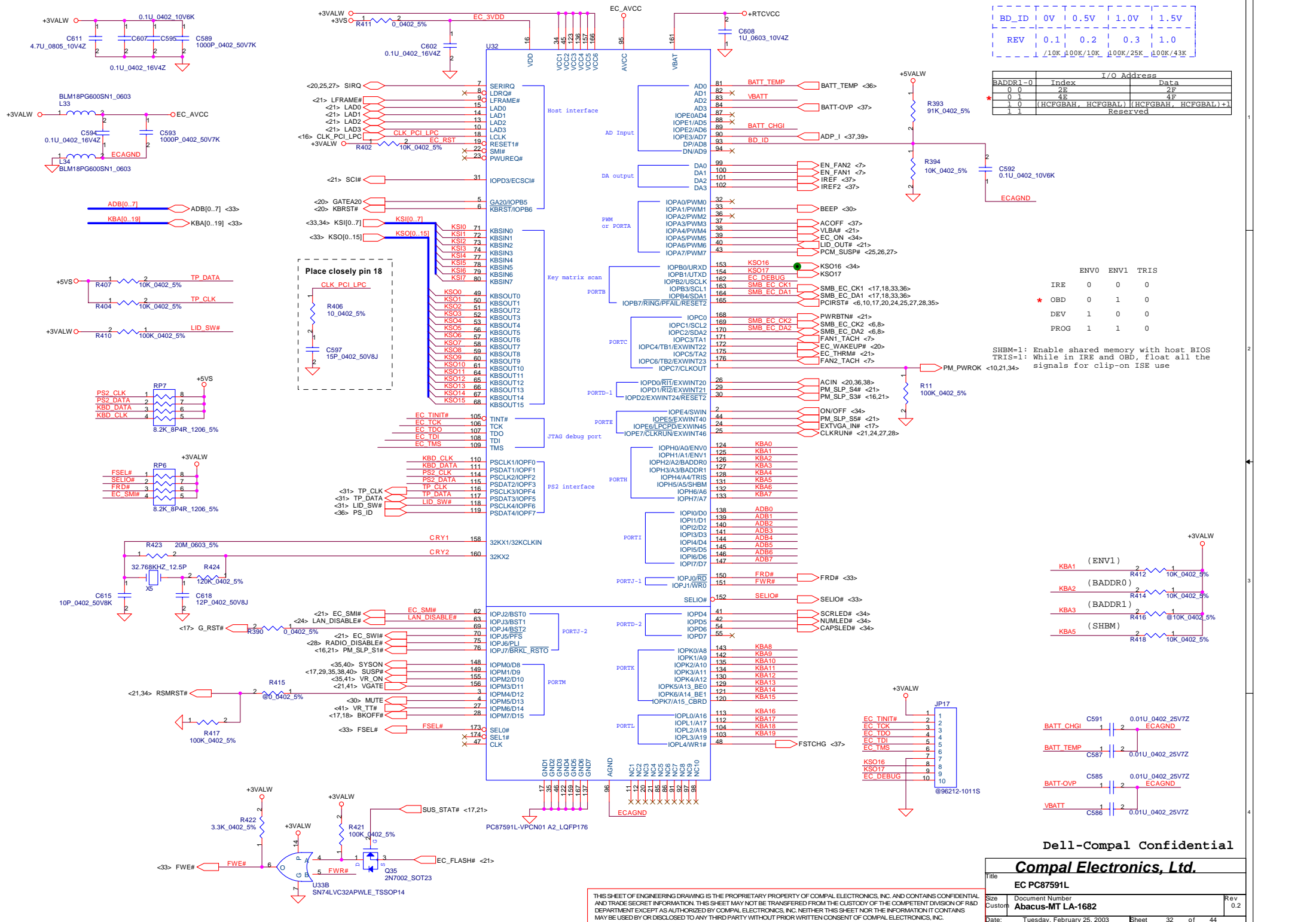


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Title		
MDC/SWITCH Connector		
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	Abacus-MT LA-1682	0.2
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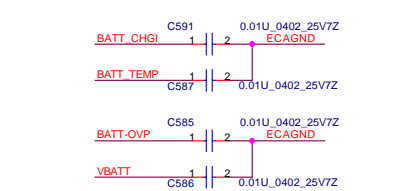
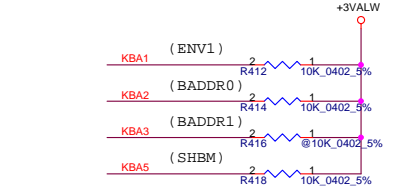


BD_ID	0V	0.5V	1.0V	1.5V
REV	0.1	0.2	0.3	1.0

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCPGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL) <1
1 1	Reserved	

ENVO	ENV1	TRIS
IRE	0	0
OBD	0	1
DEV	1	0
PROG	1	0

SHBM=1: Enable shared memory with host BIOS  
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



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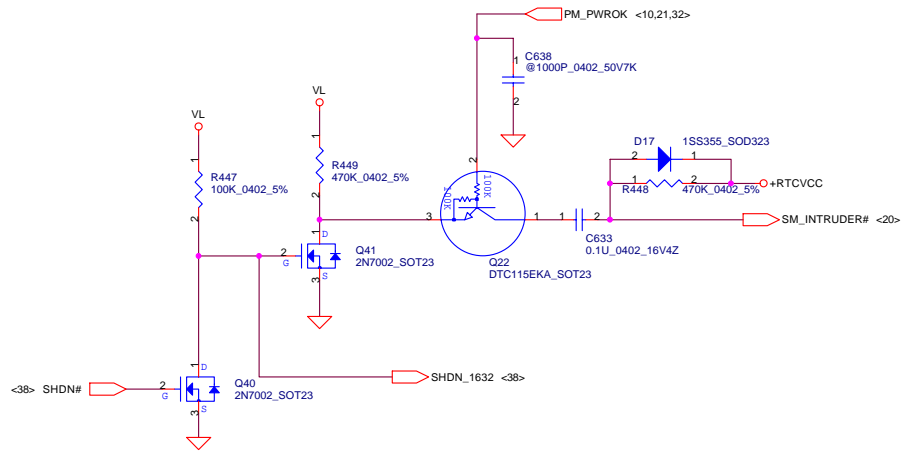
**Compal Electronics, Ltd.**  
 EC PC87591L

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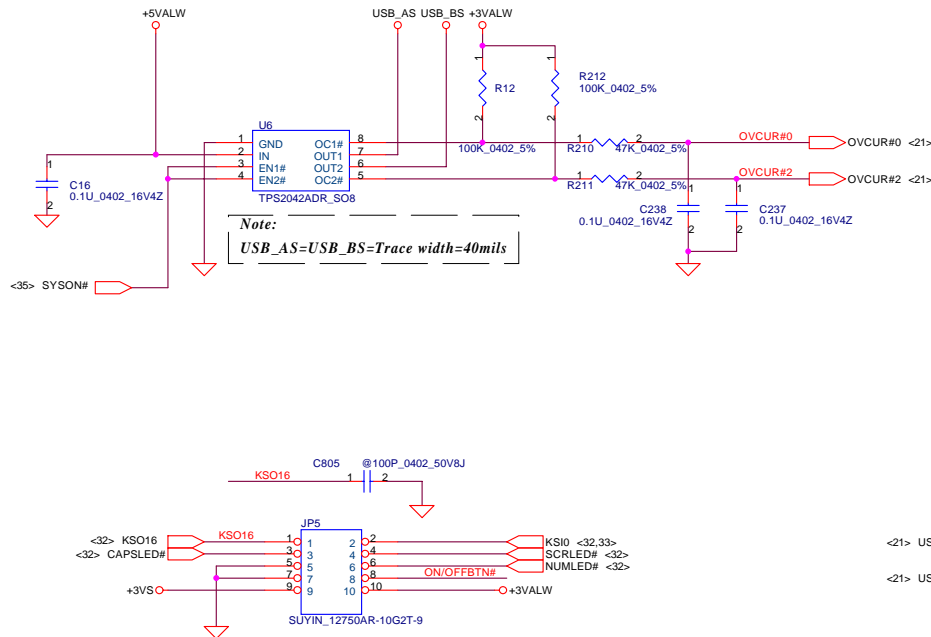
Title	EC PC87591L
Size	Document Number
Custom	Abacus-MT LA-1682
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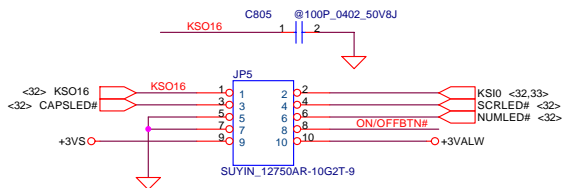




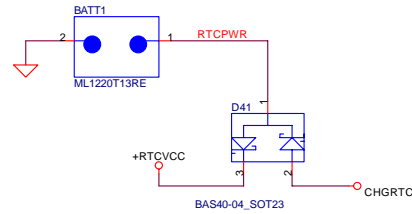
### USB Over Current



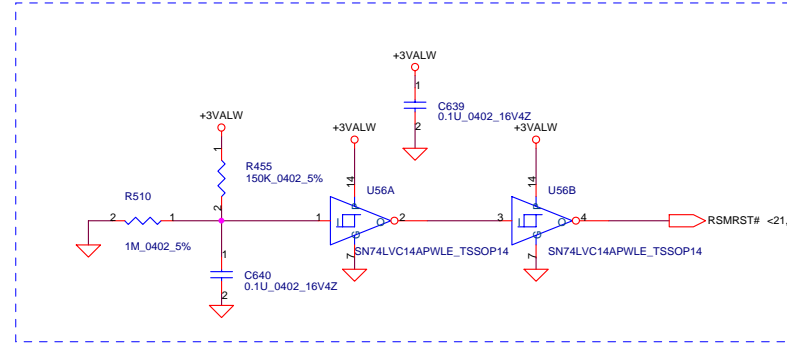
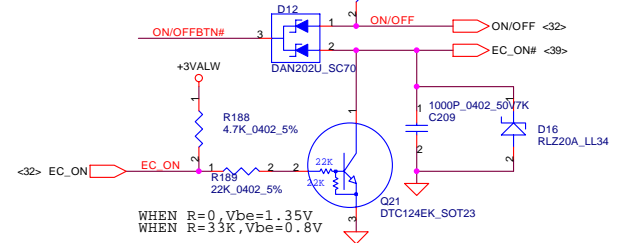
### Power SW Function Button



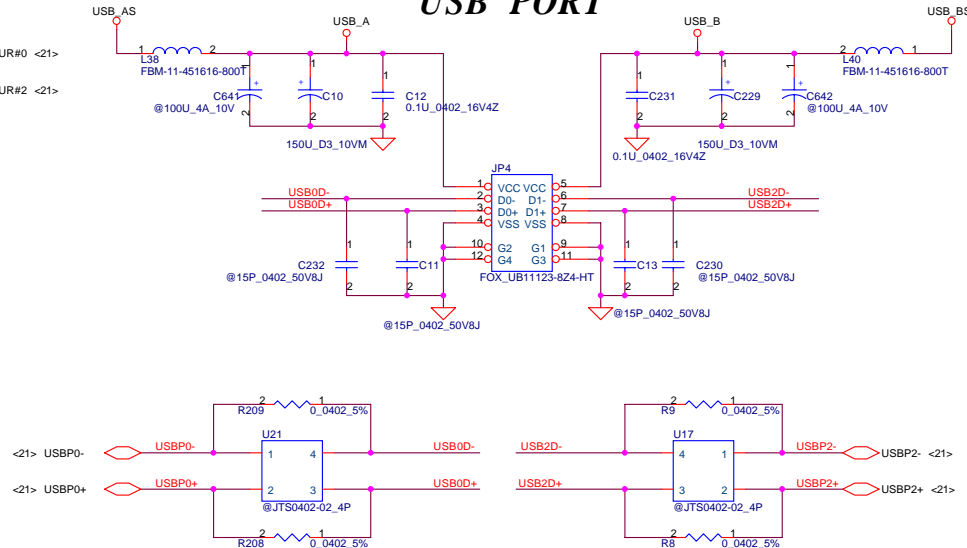
### RTC Battery



### Power BTN



### USB PORT



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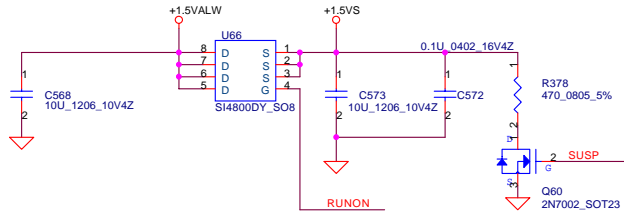
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Power OK/Reset/RTC battery/USB Conn

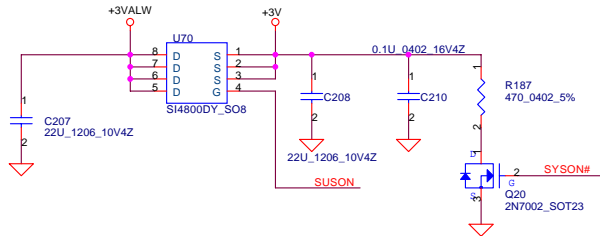
Title	Power OK/Reset/RTC battery/USB Conn	
Size	Document Number	Rev
	Abacus-MT LA-1682	0.2
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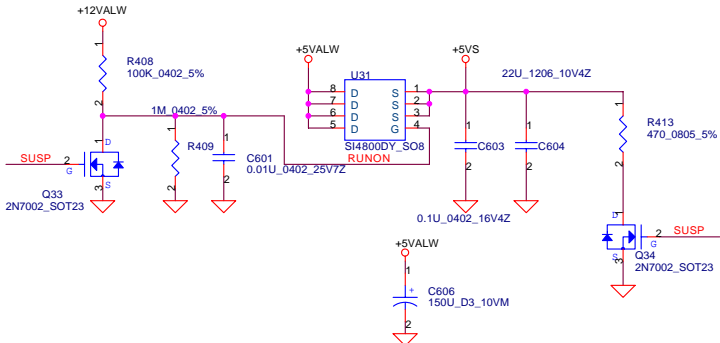
**+1.5VALW to +1.5VS Transfer**



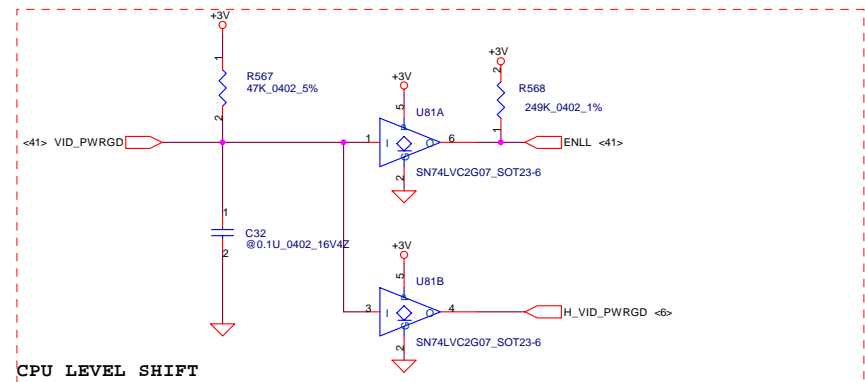
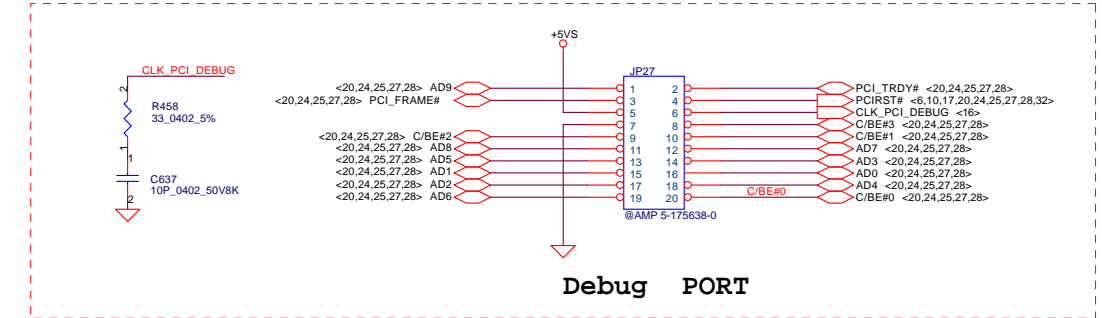
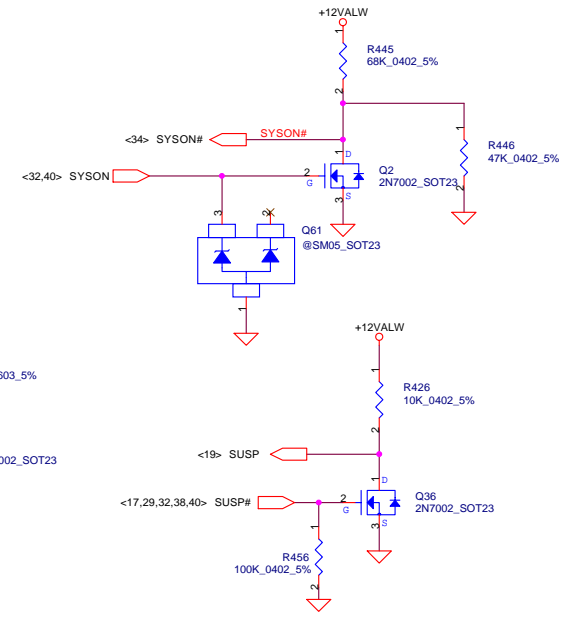
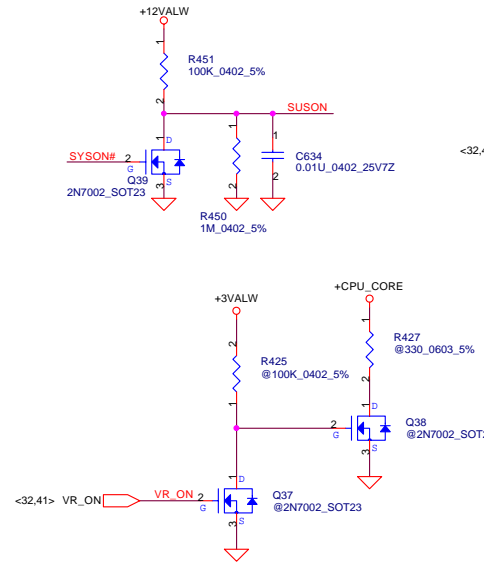
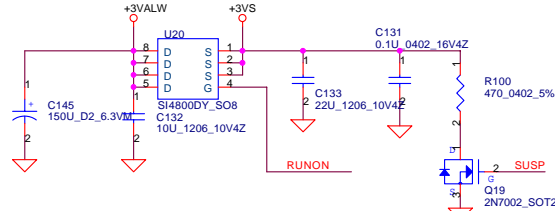
**+3VALW to +3V Transfer**



**+5VALW to +5VS Transfer**



**+3VALW to +3VS Transfer**

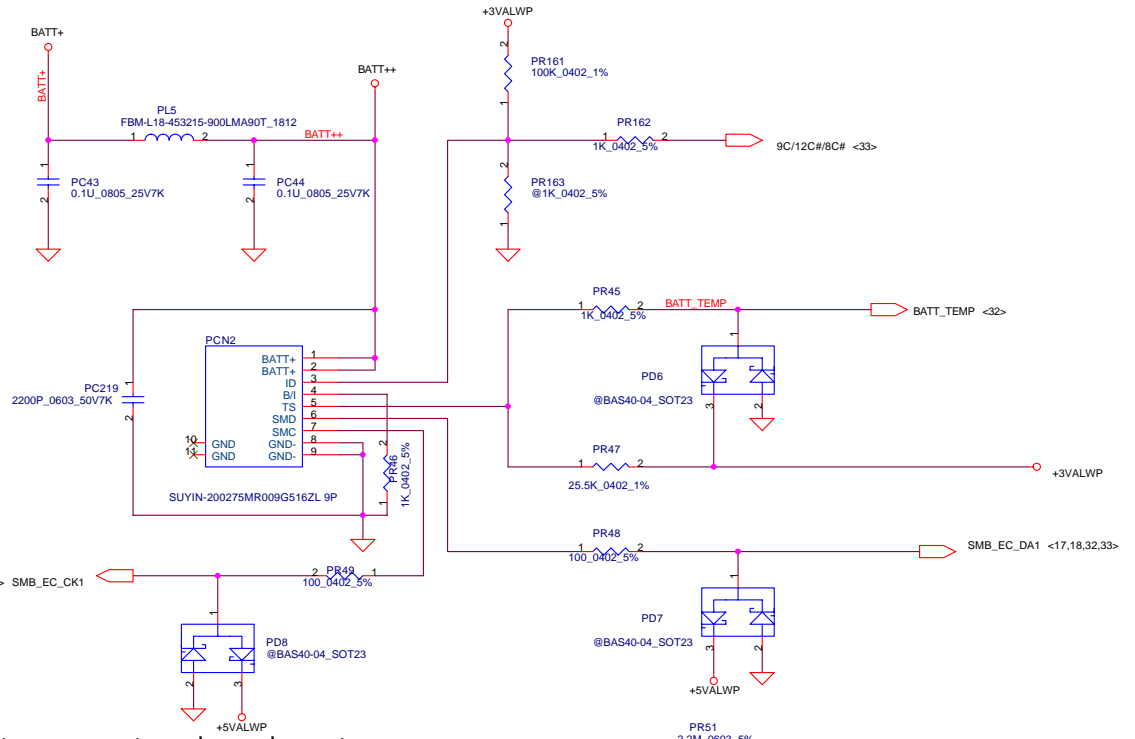
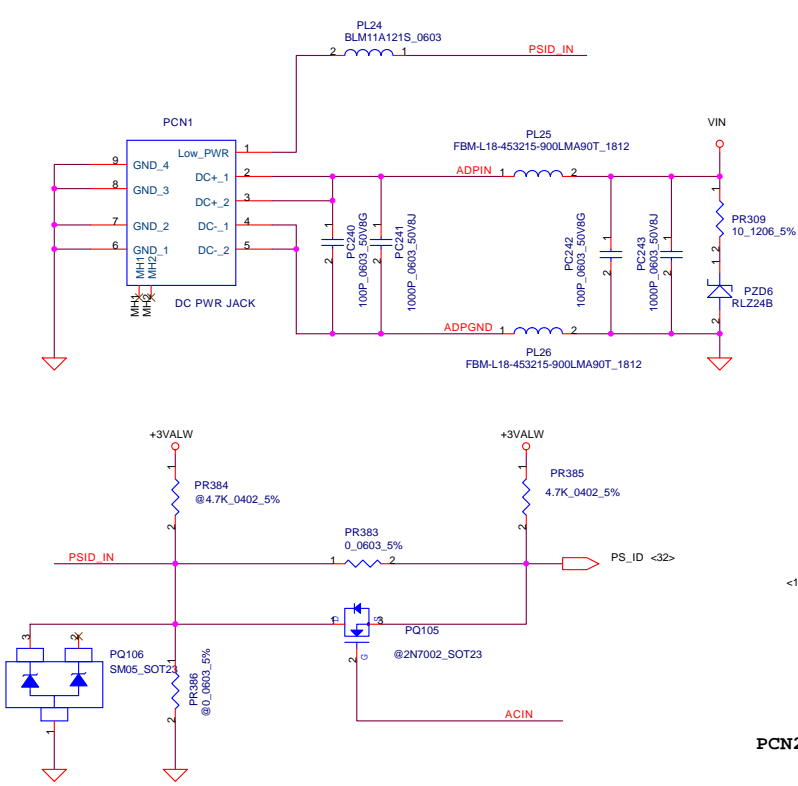


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**Compal Electronics, Inc.**

Title		
DC/DC Circuit / Debug Port		
Size	Document Number	Rev
	Abacus-MT LA-1682	0.2
Date:	Tuesday, February 25, 2003	Sheet 35 of 44

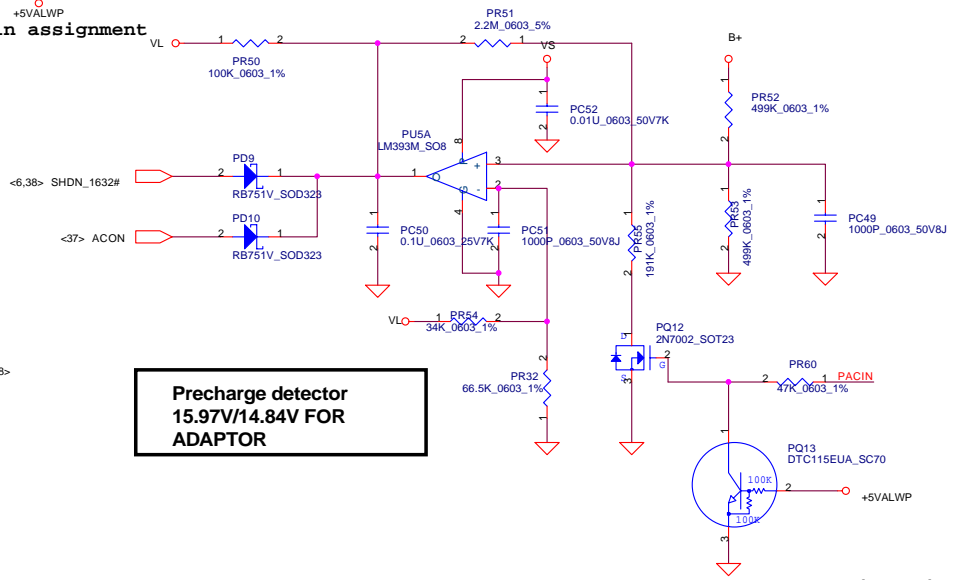
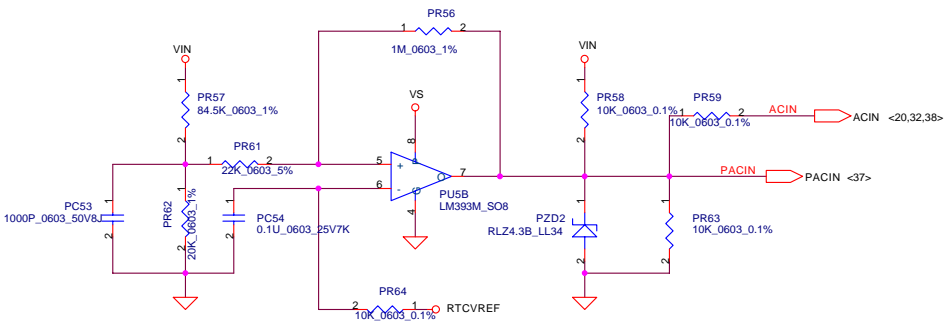
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**PCN2 battery connector pin assignment**

- SMART Battery:**
1. BATT+
  2. BATT+
  3. 9C/12C#/8C#
  4. B/I
  5. TS
  6. SMB\_EC\_DA1
  7. SMB\_EC\_CK1
  8. GND
  9. GND

**Vin Detector**  
17.90V/17.24V



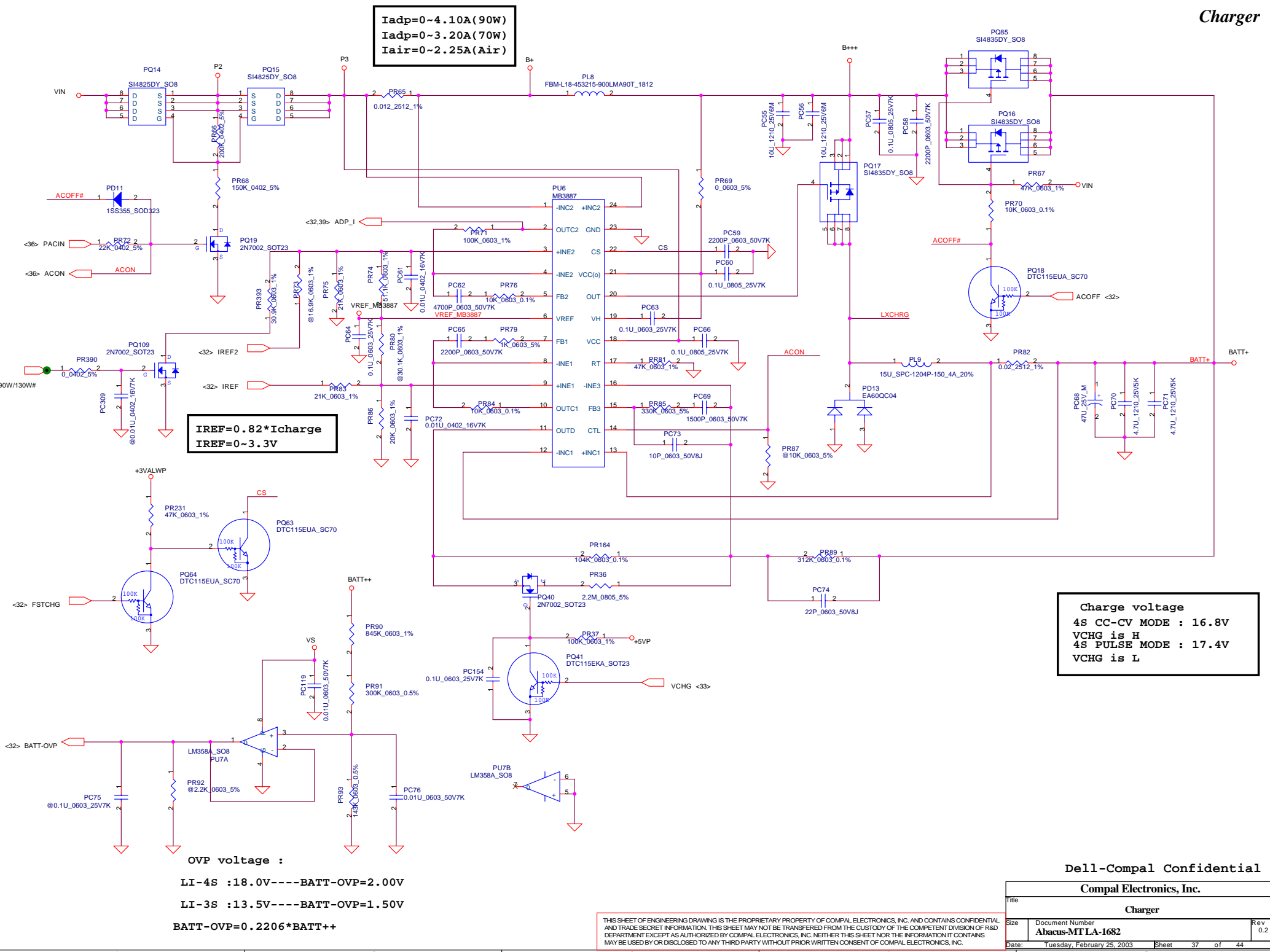
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Title		
Detector		
Size	Document Number	Rev
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**I<sub>adp</sub>=0~4.10A (90W)**  
**I<sub>adp</sub>=0~3.20A (70W)**  
**I<sub>air</sub>=0~2.25A (Air)**



**I<sub>REF</sub>=0.82\*I<sub>charge</sub>**  
**I<sub>REF</sub>=0~3.3V**

**Charge voltage**  
**4S CC-CV MODE : 16.8V**  
**VCHG is H**  
**4S PULSE MODE : 17.4V**  
**VCHG is L**

**OVP voltage :**  
**LI-4S :18.0V----BATT-OVP=2.00V**  
**LI-3S :13.5V----BATT-OVP=1.50V**  
**BATT-OVP=0.2206\*BATT++**

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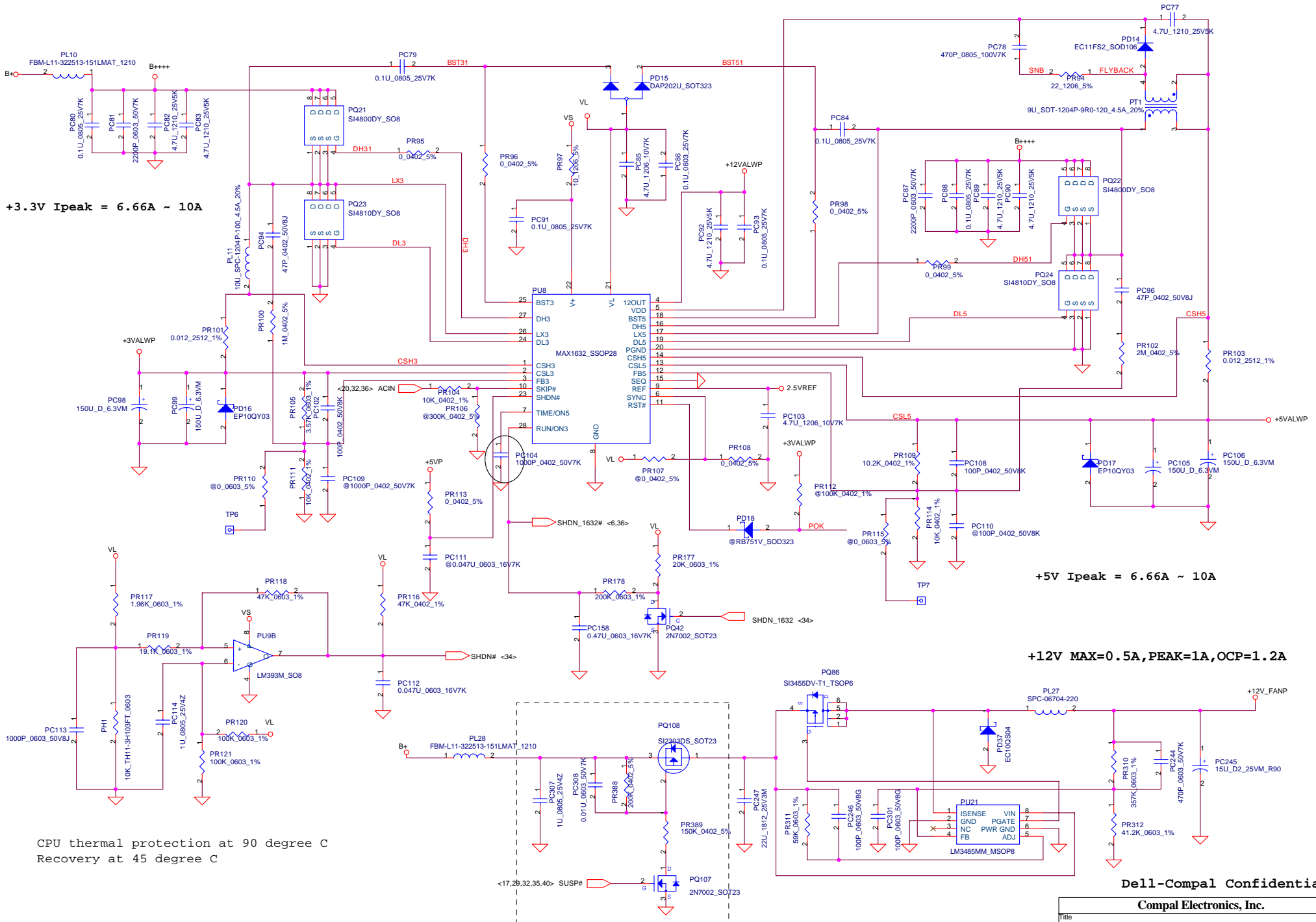
Title		
Charger		
Size	Document Number	Rev
	Abacus-MT LA-1682	0.2
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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

+12V MAX=0.5A, PEAK=1A, OCP=1.2A

CPU thermal protection at 90 degree C  
Recovery at 45 degree C

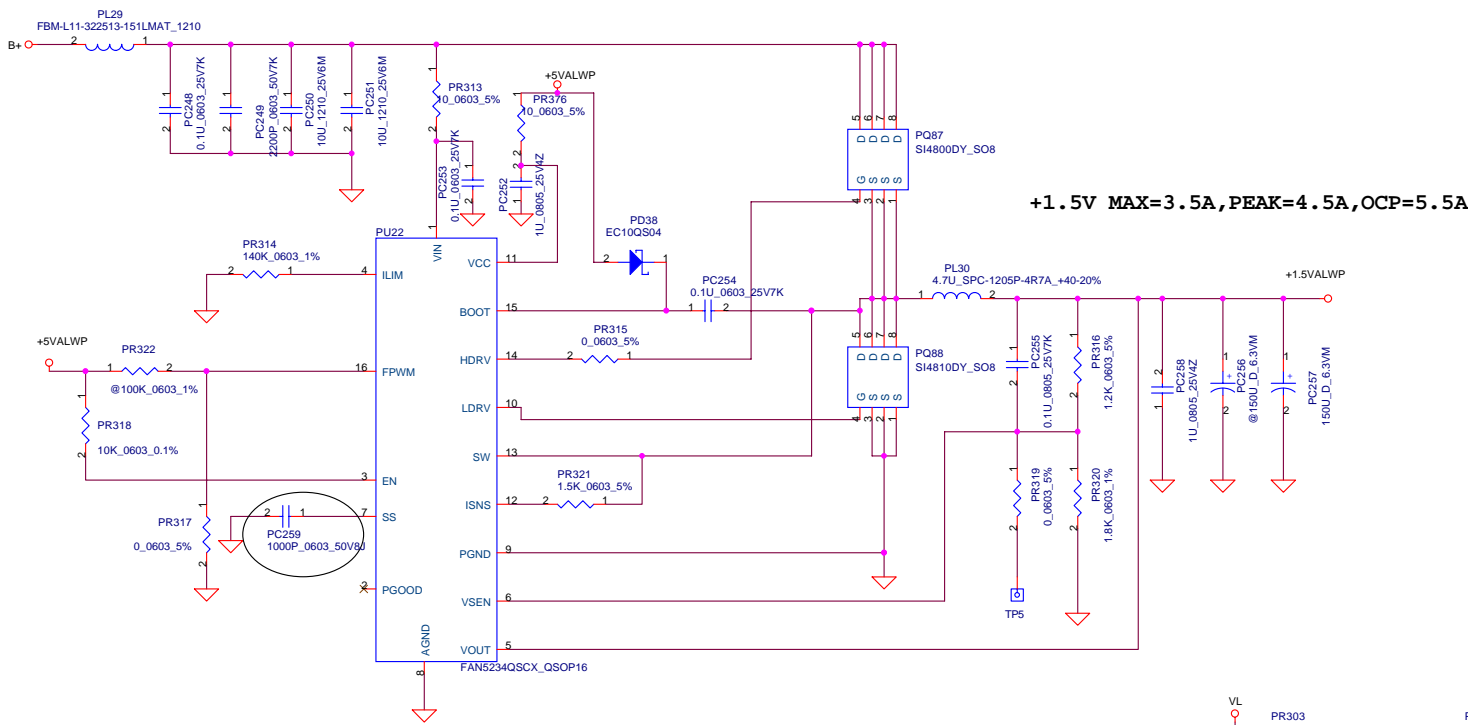


Add a switch for  
12V\_FAN on 2/11

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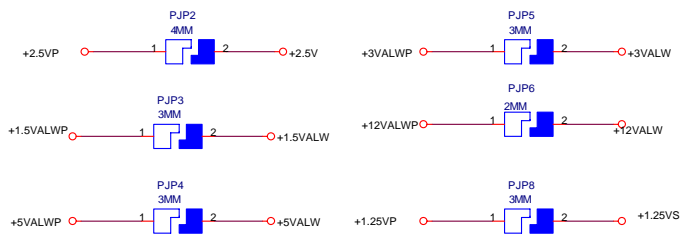
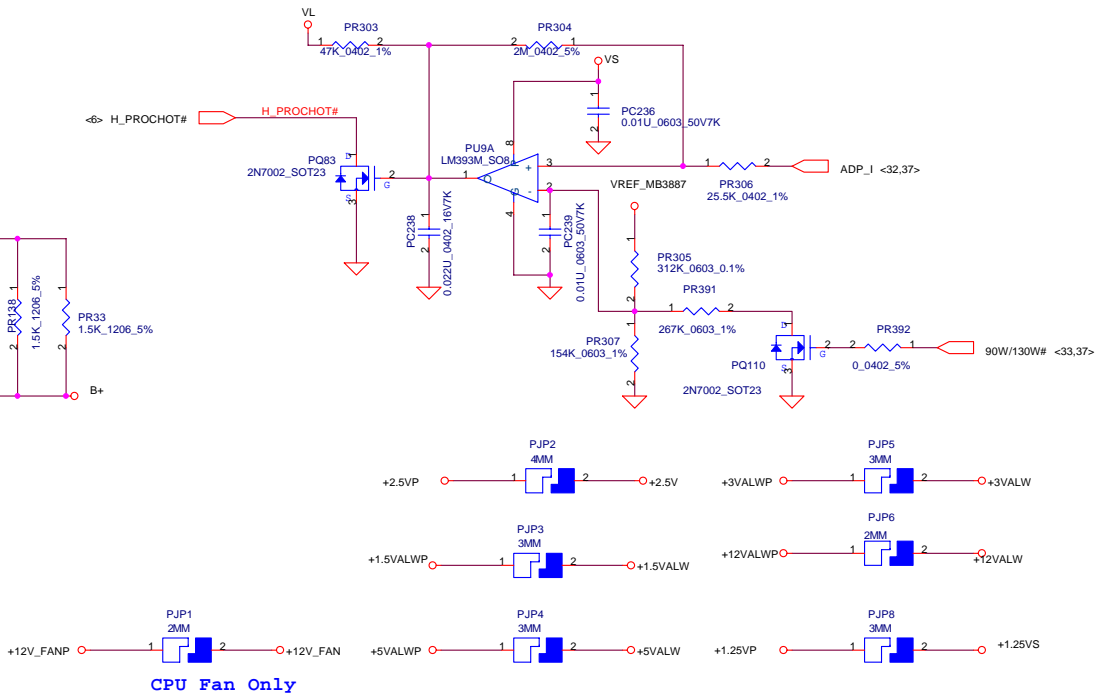
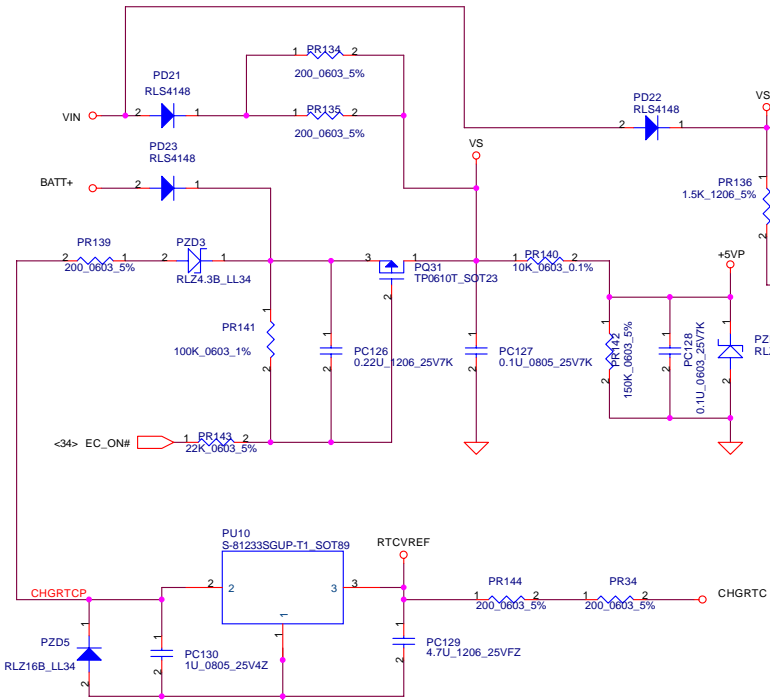
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Compal Electronics, Inc.		
Title +3.3V/+5V/+12V/+12V_FANP		
Size	Document Number Abacus-MT LA-1682	Rev 0.2
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**Adaptor Current Detector(90W)**  
 ADP\_I : 1.207V.... clock throttle(lin=5.03A)  
 ADP\_I : 1.145V....No clock throttle(lin=4.77A)

**Adaptor Current Detector(130W)**  
 ADP\_I : 1.673V.... clock throttle(lin=6.97A)  
 ADP\_I : 1.61V....No clock throttle(lin=6.71A)



CPU Fan Only

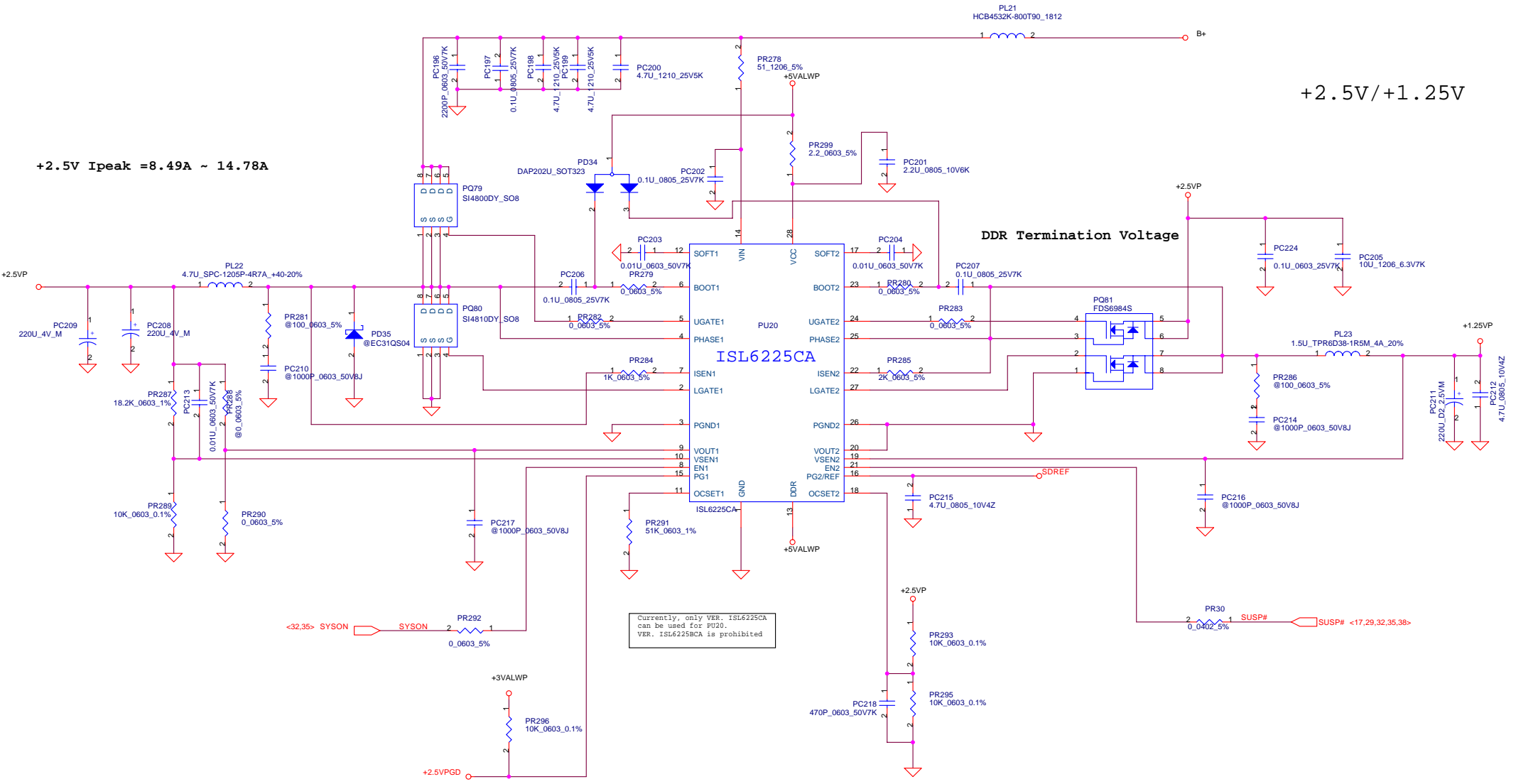
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Compal Electronics, Inc.		
Title: +1.5VS		
Size	Document Number	Rev
	Abacus-MT LA-1682	0.2
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+2.5V I<sub>peak</sub> = 8.49A ~ 14.78A

+2.5V/+1.25V

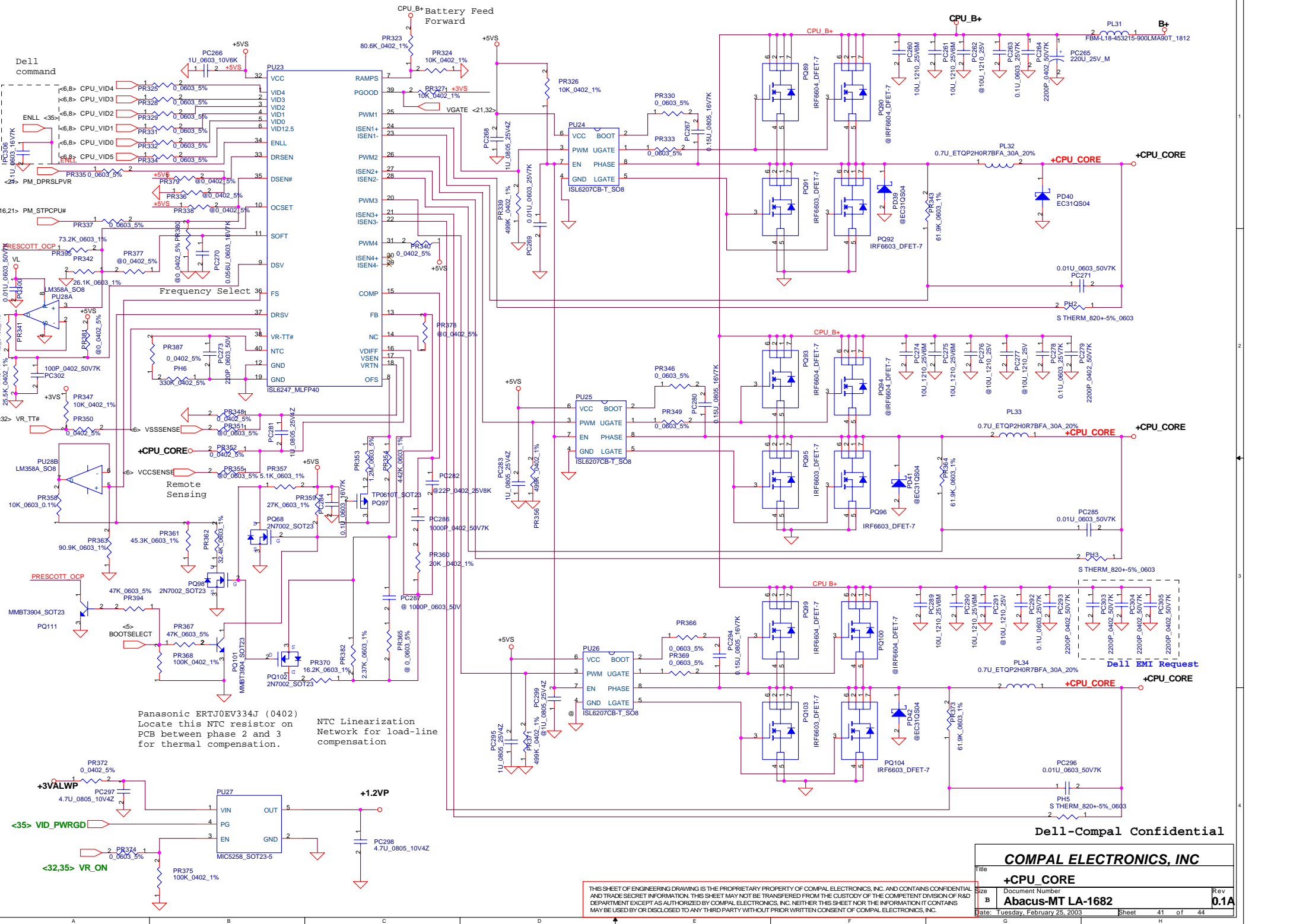


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COMPAL ELECTRONICS, INC		
Title DDR POWER 2.5V & 1.25V		
Size B	Document Number Abacus-MT LA-1682	Rev 0.2
Date Tuesday, February 25, 2003	Sheet 40 of 44	

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Dell command

RESMOTT OCP

RESMOTT OCP

<35> VID\_PWRGD  
<32,35> VR\_ON

+CPU\_CORE

Panasonic ERT07EV334J (0402)  
Locate this NTC resistor on  
PCB between phase 2 and 3  
for thermal compensation.

NTC Linearization  
Network for load-line  
compensation

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<b>COMPAL ELECTRONICS, INC</b>			
Title	<b>+CPU CORE</b>		
Size	Document Number		
B	<b>Abacus-MT LA-1682</b>		
Date:	Tuesday, February 25, 2003	Sheet	41 of 44
Rev	<b>0.1A</b>		

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**Power Version change list (P.I.R. List)**

Item	Fixed Issue	Reason for change	CKT Rev.	PG#	Modify List	B.Ver#	Phase
1	+CPU_CORE voltage error	CPU ID net error	0.1A	P41	Swap net CPU_VID0 and CPU_VID4 , CPU_VID1 and CPU_VID3(rework)	0.1	SST
2	FAN turns on when system off with battery only	need to add a switch to control 12V_FAN power when system off with battery only	0.1A	P38	add a switch for 12V_FAN with PR388 200K 5% 0402 PR389 150K 5% 0402 PC307 1uF/25V 0805 PC308 0.01uF/50V 0603 PQ107 2N7002 PQ108 SI2303DS	0.2	PT
3	doulbe pulses on the output of U81.4 when the input U81.3 slowly rises to 1.58v	for H-VID_PWRGD transtion timing with VID_PWRGD meet Intel SPEC.	0.1A	P41	change PU27 CM2843 to PU27 MIC5258	0.2	PT
4	MOSFET SMT damage	to provide MOSFET damage	0.1A	P41	Change PQ89, PQ90, PQ91, PQ92, PQ93, PQ94, PQ95, PQ96, PQ99, PQ100, PQ103, PQ104 symbol footprint	0.2	PT
5	Issue found in ISL6225BCA	Oscillation behavior found in ISL6225BCA	0.1A	P40	change PU20 from ISL6225BCA to ISL6225CA		
6	Load line is not suit Intel SPEC.	Change load line	0.1A	P41	Change PR354 from 340K to 442K and PR382 from 1.91K to 2.49K	0.2	PT
7	Adapter is 90W/130W	Detect adapter 130W/90W	0.1A	P37	Add PQ109,PR390,PC309,PR393	0.2	PT
8	Change capacitor meterial	Capacitor material is not available	0.1A	P38	Change PC245 from100U to 15U		
9	Adapter is 90W/130W	Detect adapter 130W/90W	0.1A	P39	Add PR391,PQ110,PR392,and change PR305 from 0 to 115K	0.2	PT
10	Load line test	Base on Dell power team load line test	0.1A	P41	De-pop PC282,change PR382 to 2.37K, PR361 to 45.3K,PR341 to 442 Ohm,PR344 to 25.5K,PR343,PR364,PR373 to 61.9K	0.2	PT
11	+RTCCLK and S3# will a pulse when AC plug in	delay +3VALW output	0.1A	P38	Change PC104 to 1000P	0.2	PT
12	+RTCCLK and S3# will a pulse when AC plug in	delay +1.5VALW output rise time	0.1A	P39	Change PC259 to 1000P; PD38 EC10QS04 for cost down		
13	12V FAN OCP point	Change 12V FAN OCP point,and modofy circuit	0.1A	P38	Change PR311 to 59K,PC244 to 470P, PC245 to 15uF/25V	0.2	PT
14	Issue found in ISL6225BCA	With fix PWM condition	0.1A	P40	Change PR290 to 0 and De-pop PR288	0.2	PT
15	Not easy to adjust OCP setting only, due to DVS and OCSET both within same network divider	separate OCP setting point from the DSV setting point; Particularly, use the BootSelect signal to control different OCP setting points for NW CPU and Prescott-MT CPU	0.1A	P41	Use the PU28A for DSV setting only; use PR342 26.1K for NW CPU ocp setting; for prescott-MT CPU ocp setting, add PR395 73.2K, PQ111 MMBT3904, PR394 47K, and change PR367 to 47K. Dep PR378 requested from Dell	0.2	PT
						0.2	PT
						0.2	PT

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<b>COMPAL ELECTRONICS, INC</b>		
Title <b>Power PIR</b>		
Size	Document Number	Rev
	<b>Abacus-MT LA-1682</b>	<b>0.2</b>
Date: Tuesday, February 25, 2003		Sheet 42 of 44

## H/W Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	CKT Rev.	PG#	Modify List	B.Ver#	Phase
1	System can't turn on	B+ is shutdown when AC in, Because the timing sequence of +12VALW is later than +12V_FAN	0.1A	P7	Change U76 VCC net from +12VALW to +12V_FAN(rewrite)	0.1	SST
2	H_VID_PWRGD delay time from VID_PWRGD is not enough	VID_PWRGD with H_VID_PWRGD Sequence need to meet the Intel specification (H_VID_PWRGD delay 1-10ms from VID_PWRGD)	0.1A	P35	Change R567 on BOM SD028100200 10K_0402_5% to SD028200200 20K_0402_5% and add C32 0.1U_0402_16V4Z	0.2	PT
3	Abacus and Abacus-MT K/B is different	Change K/B connector to Abacus compatible	0.1A	P33	Change K/B connector JP32 from SP01J00133L S H-CONN JAE FK2S030W11 30P to SP01F005110 S H-CONN FOXCONN GS22250-0001 25P P1 and delete the net KSO17 and C805	0.2	PT
4	LA-1682 MB INVPWR_B+ can't used the LS-1452 VGA BD	We will use the LS-1452 to BDW11/12 project, will reduce some parts for External Graphic.	0.1A	P17	Change net pin 164/166/168/170 of JP8 from INVPWR_B+ to B+ and Q71, C793, C795, R560, R562, Q74 add "1@"	0.2	PT
5	Board ID change	Board ID change for EC code, due to the KB change	0.1A	P32	Change Board ID to 0.5V ,So replace and pop the R393 with SD028910200 S RES 1/16W 91K +-5% 0402	0.2	PT
6	KB back to Abacus	JP5 pin1 signal KSO17 change to KSO16	0.1A	P34	JP5 pin1 signal KSO17 change to KSO16	0.2	PT
7	Prevent EMI impact	Prevent CLK_AGP_66M antenna impact when no used	0.1A	P17	Add R17 1@33_0402_5% (SD028330A00 S RES 1/16W 33 +-5% 0402) And C33 1@10P_0402_25V8K (SE068100K00 S CER CAP 10P 25V +-10% NPO 0402)	0.2	PT
8	Lan EEPROM Material control	U8 will used the eeprom same as Abacus	0.1A	P24	Change the BOM U8 from SA093461030 without LAN code to SA093461040 with Abacus LAN code	0.2	PT
9	Extra connector	Jp33 just for A-test BIOS debug connector	0.1A	P33	Remove Jp33 on BOM	0.2	PT
10	RTCCLK ringback	Need to add series termination on RTCCLK at the ICH because of signal quality/undershoot and ringback at Q69	0.1A	P21	Add R18 SD028220A00 S RES 1/16W 22 +-5% 0402 and C62 SE068101K00 S CER CAP 100P 25V +-10% NPO 0402	0.2	PT
11	Part Number error	Correct U77 A2 revision Part Number	0.1A	P21	Change the BOM U77 from SA243500000 S IC R682G4350M A1 UFCBGA-732 MONTARA-GT to SA828520100 S IC R682852GME A2 UFCBGA-732 MONTARA-GT.	0.2	PT SST
12	Reversed the capacitor about RTCCLK circuit	Just do the reserved the RTCCLK modify waveform cap.	0.1A	P21	Depop the C62 (add @ )	0.2	PT
13	Extra Pads about @C659 & @C660	Remove capacitor @C659 & @C660 extra component from PCB because we have not used.	0.1A	P7	Depop the parts C659 & C660 from Circuit & PCB	0.2	PT
14	H_VID_PWRGD waveform have negative pulse after rise up at VID_PWRGD voltage at 1.58V(riseing)	H_VID_PWRGD waveform abnormal	0.1A	P35	Change R567 on BOM from SD028200200 20K_0402_5% to SD028470200 10K_0402_5% and pop C32 0.1U_0402_16V4Z	0.2	PT
15	Default the ITPCLK/ITPCLK# to Intel circuit specification.	For meet Intel specification	0.1A	P6	Add @ to RP61 and add SD014499A09 49.9 +-1% 0603 R572/R573 for ITPCLK/ITPCLK# pull down	0.2	PT
16	Audio cost reduction from Dell request	Cost reduction	0.1A	P29 P30	Depop the parts C481, C554, C551 C553, C483, C622, C623, C624 change from 1uF to 0.1uF	0.2	PT
17	Improve audio performance	Improve audio performance	0.1A	P29	Populate C490 1uF	0.2	PT
18	Investigate Beep circuit cost down	Cost	0.1A	P30	Add R132 0 ohm, but depop. Test at PT step	0.2	PT
19	Fix HP plug in phonejack delay time	Plug in External SPK will delay some timing	0.1A	P30	C588 change from 4.7uF_0805 to 0.47uF_0603, and depop C580	0.2	PT
20	Reversed the capacitor about Fan circuit	C687 & C701 make the voltage leakage so depop the parts .	0.1A	P7	Depop the parts C687,C701 (add @ )	0.2	PT
21	1394 can not link at 400 speed.	Improve 1394 link test by TI test tool	0.1A	P25	Depop C223, C216, R198, R197, R196, R194, R199 add C822(270P), C823(1uF), R574(5.1K), R575-R578(56.2)	0.2	PT

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