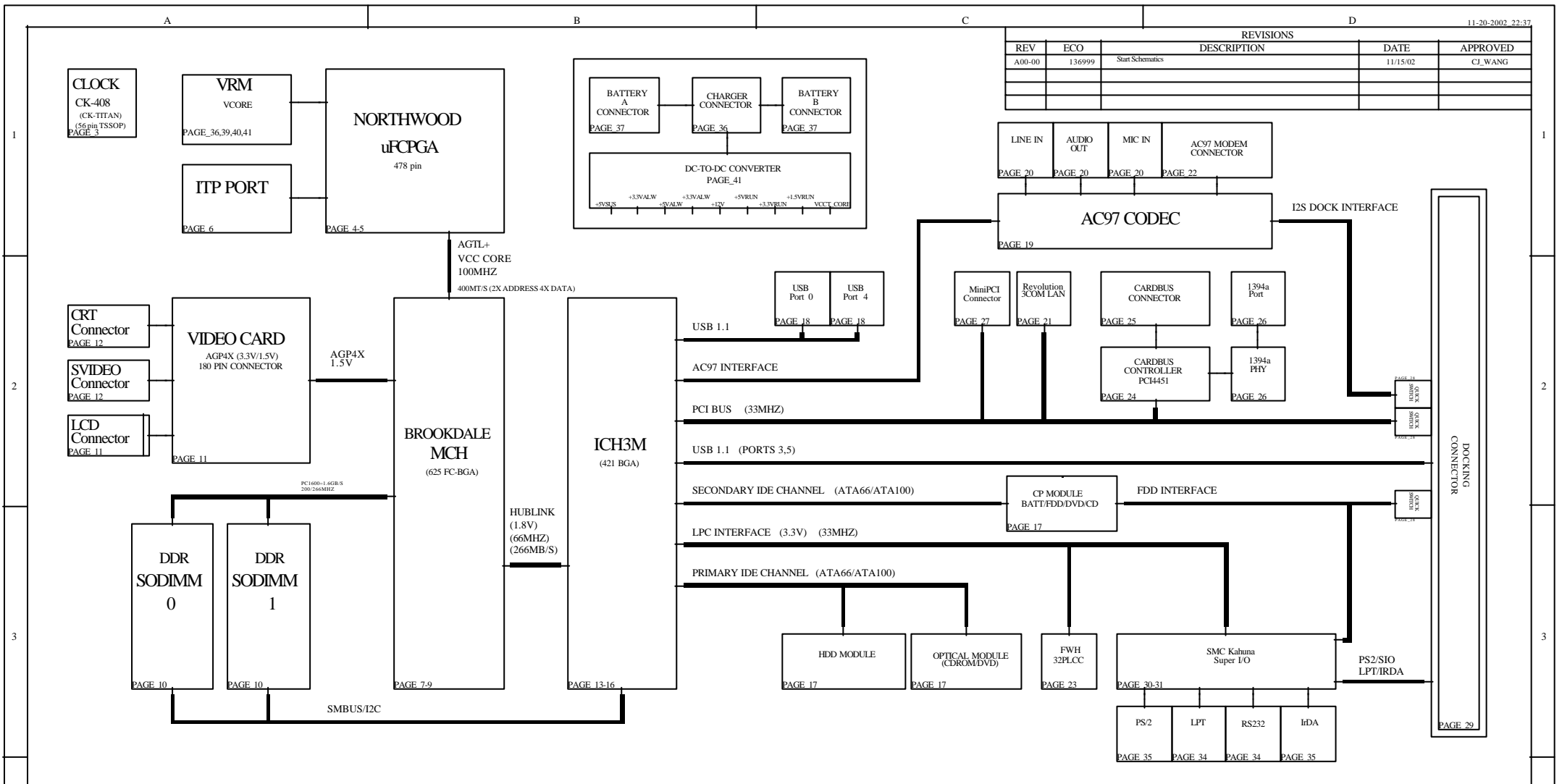


REVISIONS				
REV	ECO	DESCRIPTION	DATE	APPROVED
A00-00	136999	Start Schematics	11/15/02	CJ_WANG



PARTS

- ASSY.PWA.MN.NV28.M50 (9Y422)
- └ PWA.PLN.MN.NV28.M50 (9Y422)
 - └ ASSEMBLY BARCODE LABEL (XXXXXX)
 - └ ASSEMBLY REVISION LABEL (XXXXXX)
 - └ ASSY.DWG.PLN.MN.NV28.M50 (XXXXXX)
 - └ PWB.PLN.MN.CABN (1Y802)
 - └ SCHEM.PLN.MN.NV28.M50 (C0370)

BOM ADDS APPEAR ON PAGE 42.

- This design requires a font mapping of Fixed to scalable Arial with a scaling factor of 1.0
- Please remember when copying project files that you must include both the symbols and the schematics

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M50 A00

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DELL COMPUTER CORPORATION AUSTIN, TEXAS

TITLE: SCHEMATIC, M/B LA-1221

PWG NO: 40195 REV: 4A

DATE: 11/15/02 SHEET: 52 OF 102

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2. Index
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34. Parallel and Serial Ports
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45. SMBUS Diagram
- 46-50. REFDES Page Index

NEEDS TO BE UPDATED

POWER MODES

Power Mode	Voltage	Page	Source	ON	OFF
RBAT	7.2V	32, 36		Always	
PBATT+	1.7V-13V	36, 37, CB - 3		Always	
SBATT+	1.7V-13V	36, 37, CB - 3		Always	
DOCK_DC_IN	20V	29, 36		Always	
DC_IN	20V	29, 36, CB - 2, 3		Always	
SDC_IN	20V	CB - 2, 3		Always	
V_CHG	15V-17.5V	CB - 2		Note 1	
PWR_SRC	7.2V-20V	8, 11, 29, 36, 38, 39, 40, 41		Always	
RTC_SRC	7.2V-20V	36, 39		Always	
3VSUS	3.3V	4, 6, 10-16, 18, 21-25, 27, 30-31, 35, 38-41		S1-S3	S4-S5
RTC_PWR	5V	36, 38, 39, 41, 42		Always	
5VSUS	5V	8, 11, 16, 18-19, 22, 25, 29, 33-35, 38-42		S1-S3	S4-S5
2.5VSUS	2.5V	8, 10, 39		S1-S3	S4-S5
VCC_CORE	0.6V-1.75V	4, 5, 9, 16, 23, 38, 40		S1-S2	S3-S5
12V	12V	3, 11, 25, 29, 33, 36, 38, 41		S1-S2	S3-S5
DOCK_PWR_SRC	13V-20V	29	Docked ALW		
3VRUN	3.3V	3, 4, 6, 11, 13-14, 16-17, 19, 21-23, 26-28, 30-31, 33, 35, 38		S1-S2	S3-S5
VAUX	3.3V	27	Note 2	Note 2	
1.8VSUS	1.8V	16, 38, 39		S1-S3	S4-S5
1.8VRUN	1.8V	7, 8, 9, 13, 16, 38		S1-S2	S3-S5
5VRUN	5V	6, 11-12, 16-17, 20, 27-28, 30, 32-35, 38, 42		S1-S2	S3-S5
5VHDD	5V	17, 38		S1-S2	S3-S5
5VMOD	5V	17, 38		S1-S2	S3-S5
1.5VRUN	1.5V	7, 9, 11, 38, 39		S1-S2	S3-S5
STRB_5V	5V	29, 34, 38		S1-S2	S3-S5
VBEHCG	0.7V	11		S1-S2	S3-S5
V_IP2SV_DDR_VTT	1.25V	8, 10, 11, 38, 39		S1-S2	S3-S5
CRF_VCC	5V	12		S1-S2	S3-S5
SV_ODOCK	5V	28, 30		S1-S2	S3-S5
5VEDDPP	5V	17, 31, 38		S1-S2	S3-S5
5VSUS_DOCKED	5V	29	Docked S1-S3	Docked S4-S5	
USB_PWR_04	5V	18		S1-S2	S3-S5
VDDA	4.65V	19, 20		S1-S2	S3-S5
VDDA2	2.5V	19, 20		S1-S2	S3-S5
1.2V_VCCVID	1.2V	4, 40		S1-S3	S4-S5
5VALW	5V	11, 29, 30-32, 35-37, 39, 41		Note 4	Note 4
3VVRTC	3.3V	16, 31, 36, 39, 41		Always	
3VALW	3.3V	6, 17, 30, 32, 35, 36, 39, 41		Note 4	Note 4
VCC_RTC	3.3V	14, 16		Always	
ICH_VBIAS	3.3V	14, 16		S1-S2	S3-S5
3VPHYD	3.3V	26		S1-S2	S3-S5
3VPHYA	3.3V	26		S1-S2	S3-S5
CK_VDD_MAIN	3.3V	3		S1-S2	S3-S5
CK_VDD_CORE	3.3V	3		S1-S2	S3-S5
V_3P3_LAN	3.3V	21, 22		S1-S3	S4-S5
V_3P3_LAN_VDDTX	3.3V	21		S1-S3	S4-S5
V_3P3_LAN_VDDRX	3.3V	21		S1-S3	S4-S5
V_MCH_GTLREF	0.675VCC_CORE	8		S1-S2	S3-S5
S1_VPP	0V-12V _{Note A}	25		S1-S3	S4-S5
S2_VPP	0V-12V _{Note A}	25		S1-S3	S4-S5
S1_VCC	0V-5V _{Note A}	24, 25		S1-S3	S4-S5
S2_VCC	0V-5V _{Note A}	24, 25		S1-S3	S4-S5
S1_VCCF	0V-5V _{Note A}	24, 25		S1-S3	S4-S5
S2_VCCF	0V-5V _{Note A}	24, 25		S1-S3	S4-S5
HL_REF	0.9V	8, 13		S1-S2	S3-S5
H_VCCA	1.2V	4		S1-S3	S4-S5
H_VCCIOPLL	1.2V	4		S1-S3	S4-S5
H_GTLREF	0.675VCC_CORE	4		S1-S2	S3-S5
H_VSSA	1.2V	4		S1-S3	S4-S5
V_DDR_MCH_REF	1.25V	8, 10, 39		S1-S3	S4-S5

Note A Voltage delivered to these pins is determined from the type card inserted to the PCMCIA controller.

Note 1 Rail is available anytime AC and BATTERY are both present, and the BIOS is not inhibiting charge

Note 2	NB powered by AC	VAUX	S1-S3	S4-S5
	NB powered by BATT	VAUX	S1-S2	S3-S5

Note 3 Rail is available anytime the HEADPHONE Jack is occupied

Note 4	NB powered by AC	3VALW	Always	
	NB powered by BATT	3VALW	S1-S3	S4-S5
	NB powered by AC	5VALW	Always	
	NB powered by BATT	5VALW	S1-S3	S4-S5

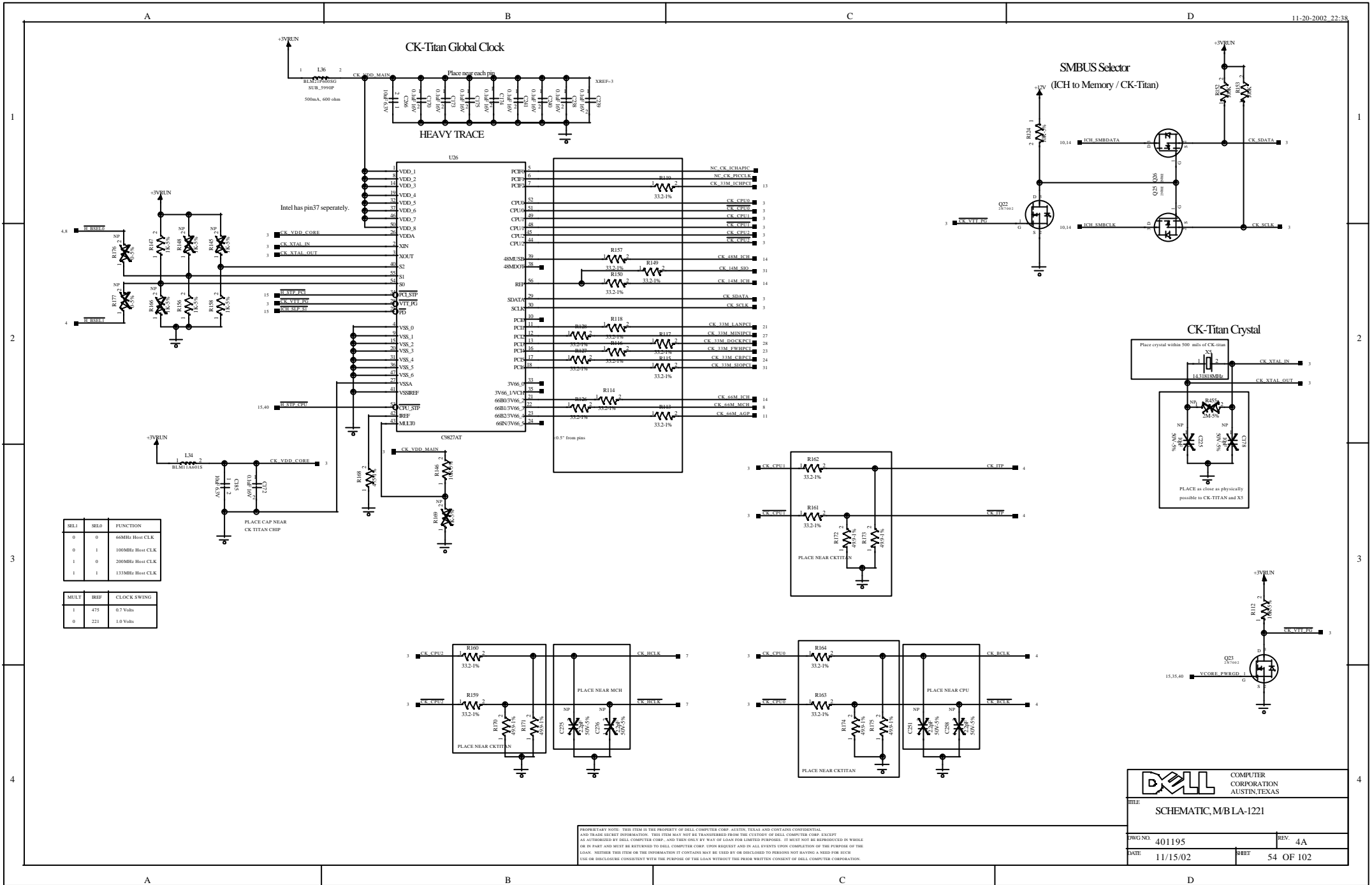
PCI TABLE

DEVICE	IDSEL	IRQ	REQ/GNT	DREQ/DGNT
DOCK	AD24	PIRQC*		REQ0*/GNT0*
3COM	AD16	PIRQC*		REQ4*/GNT4*
VIDEO	IDSEL	PIRQA* PIRQB*		
PCI4451	AD17	PIRQD*	REQB*/GNTB*	REQ1*/GNT1*
Msi	AD18	PIRQA*	REQA*/GNTA*	REQ2*/GNT2*
MINIPCI	AD19	PIRQB* PIRQD*		REQ3*/GNT3*

BOM BUILD OPTIONS	
Option	Description
0	Base Build
1	FDD_PP

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DWG NO. 401195		REV. 4A	
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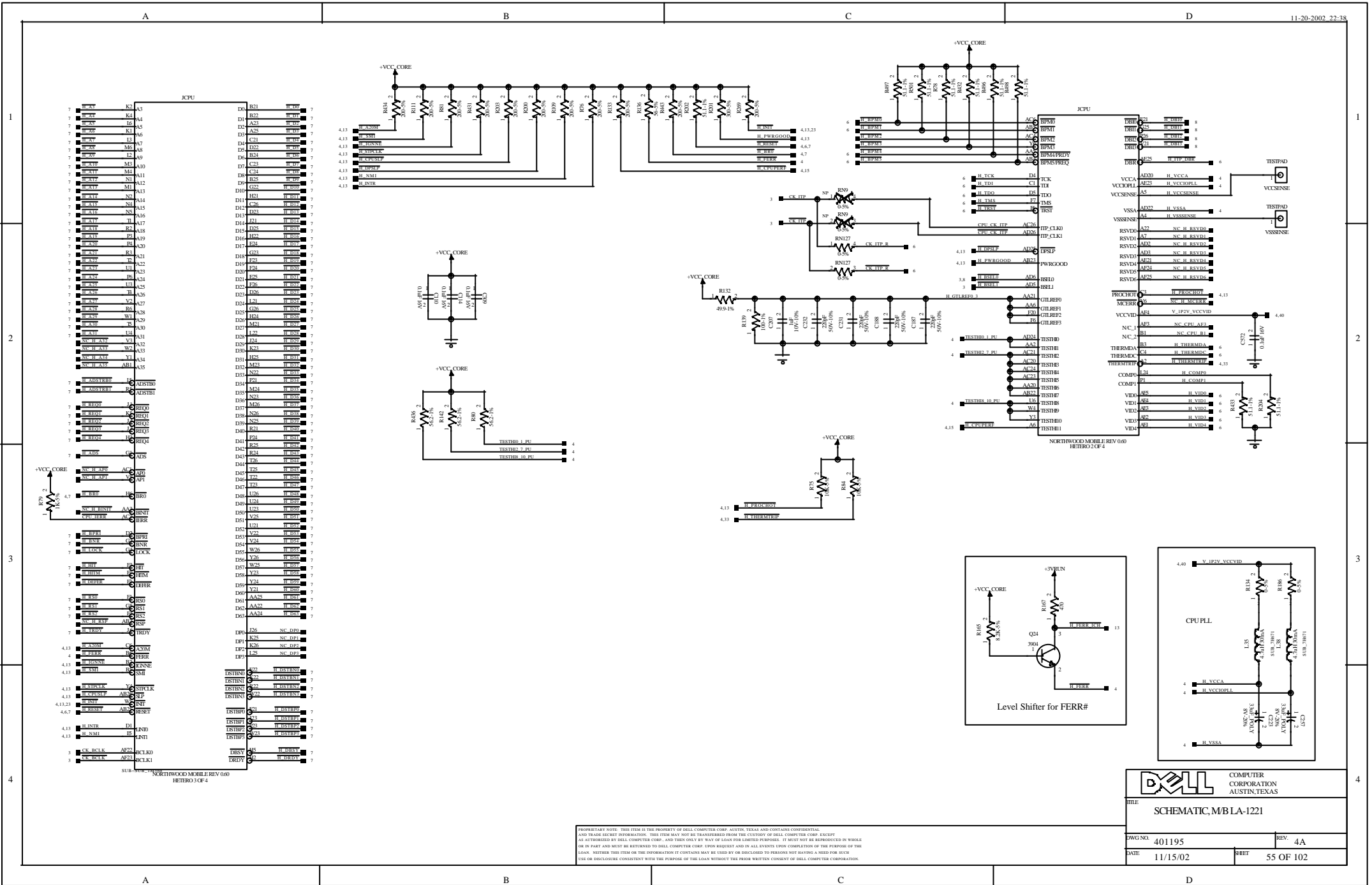
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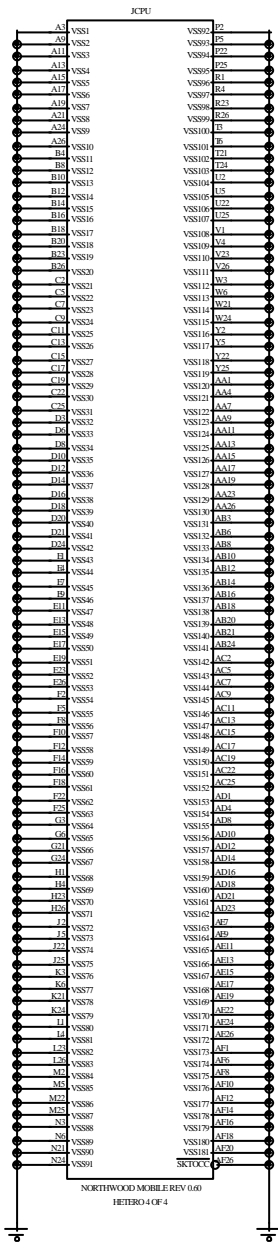
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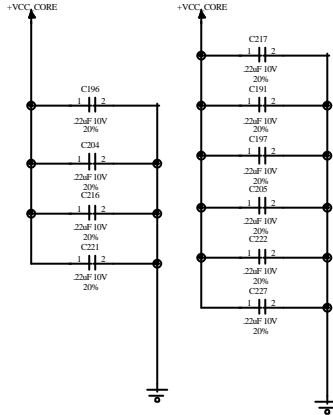


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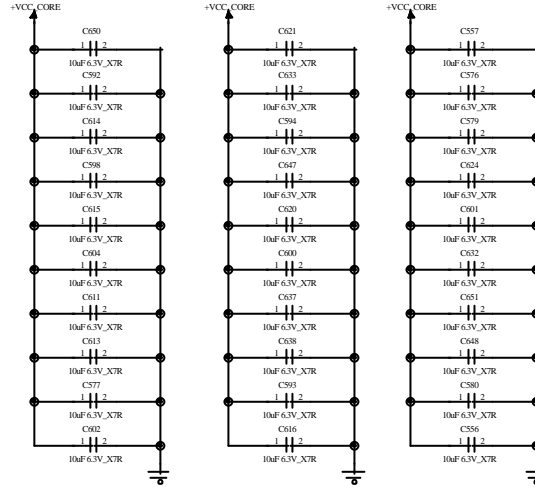
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DATE 11/15/02	SHEET 55 OF 102		



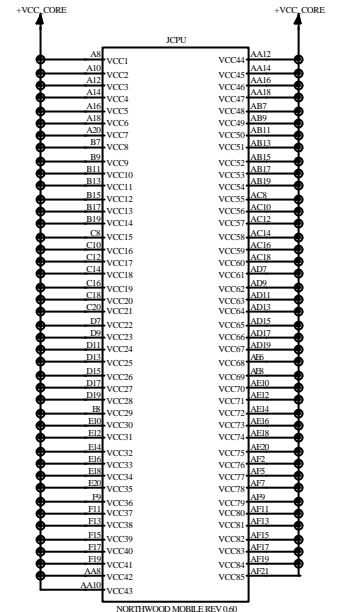
CPU High Frequency Decoupling



CPU Bulk Decoupling



Place caps close to JCPU
ALL CAPS NEED TO BE PLACED
DIRECTLY UNDER JCPU WHEN
POSSIBLE USE TWO VIAS/PAD



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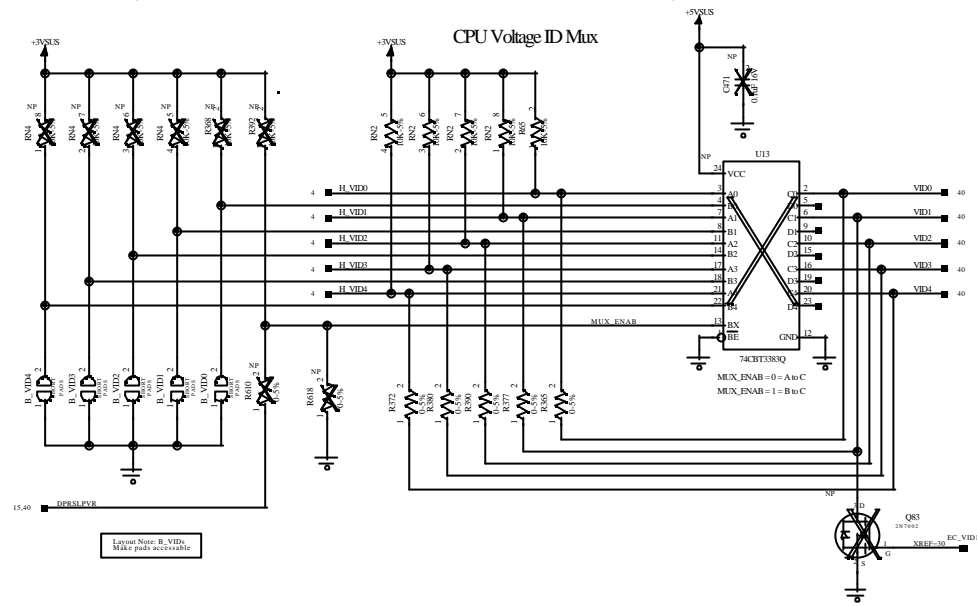
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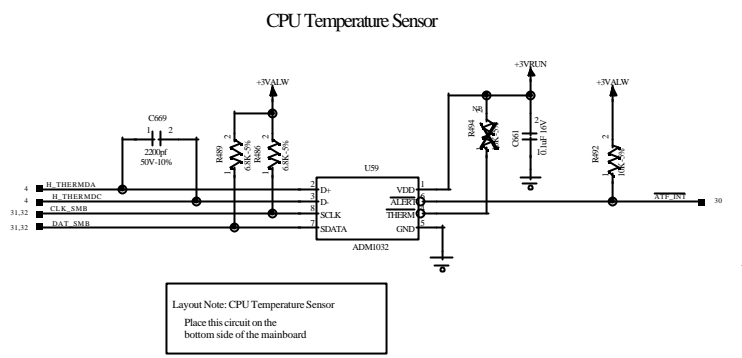
4

O = pads open
S = pads shorted

B_VID Settings				B_VID Settings							
4	2	2	1	0	VCC_CORE	4	2	2	1	0	VCC_CORE
S	S	S	S	S	1.750V	O	S	S	S	S	0.9750V
S	S	S	S	S	1.700V	O	S	S	S	S	0.950V
S	S	S	S	S	1.650V	O	S	S	S	S	0.925V
S	S	S	S	S	1.600V	O	S	S	S	S	0.900V
S	S	S	S	S	1.550V	O	S	S	S	S	0.875V
S	S	S	S	S	1.500V	O	S	S	S	S	0.850V
S	S	S	S	S	1.450V	O	S	S	S	S	0.825V
S	S	S	S	S	1.400V	O	S	S	S	S	0.800V
S	S	S	S	S	1.350V	O	S	S	S	S	0.775V
S	S	S	S	S	1.300V	O	S	S	S	S	0.750V
S	S	S	S	S	1.250V	O	S	S	S	S	0.725V
S	S	S	S	S	1.200V	O	S	S	S	S	0.700V
S	S	S	S	S	1.150V	O	S	S	S	S	0.675V
S	S	S	S	S	1.100V	O	S	S	S	S	0.650V
S	S	S	S	S	1.050V	O	S	S	S	S	0.625V
S	S	S	S	S	1.000V	O	S	S	S	S	0.600V

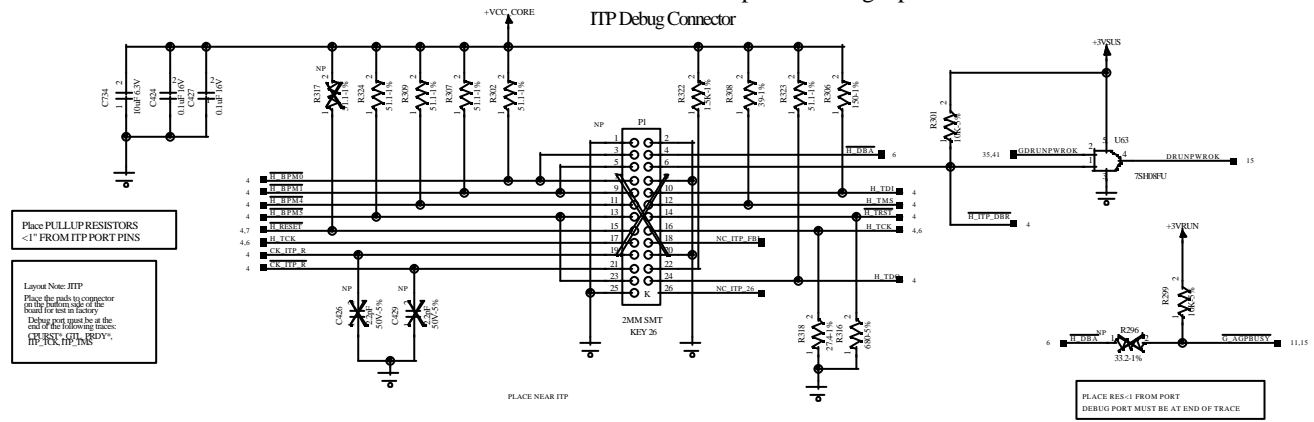


Layout Note: B_VID, MUX pads accessible



Layout Note: CPU Temperature Sensor
Place this circuit on the bottom side of the mainboard

Circuit Not Complete. Pending input from Intel.
ITP Debug Connector



Place PULL-UP RESISTORS <1> FROM ITP PORT PINS

Layout Note: ITP
Place the pads to connector on the bottom side of the board for test in factory.
Delivery open at the end of the following traces:
Destructive CPU operation:
ITP_RX, ITP_TX

PLACE NEAR ITP

PLACE RES-1 FROM DEBUG PORT MUST BE AT END OF TRACE

ITP Population Matrix

Ref. Des.	ITP Used	ITP Not Used
R264	510 ohms	1.5k
R255	pop	no pop
R257	pop	no pop
R265	no pop	1k pull-down
R258	pop	no pop
R140 (p.7)	pop	no pop
R249	pop	no pop
R248	pop	no pop
R280	no pop	no pop
R281	pop	no pop
R279	pop	no pop
R278	pop	no pop
R283	pop	no pop
R275	pop	no pop
R273	pop	no pop
R256	39 ohms	1k
R251	no pop	pop
R271	pop	no pop
R263	pop	no pop
R272	pop	pop

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A B C D

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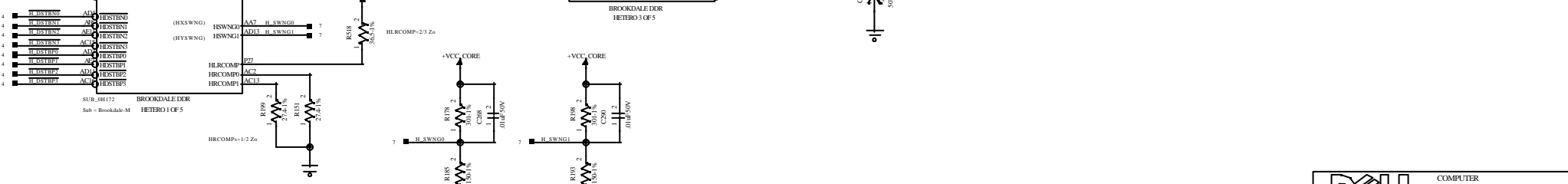
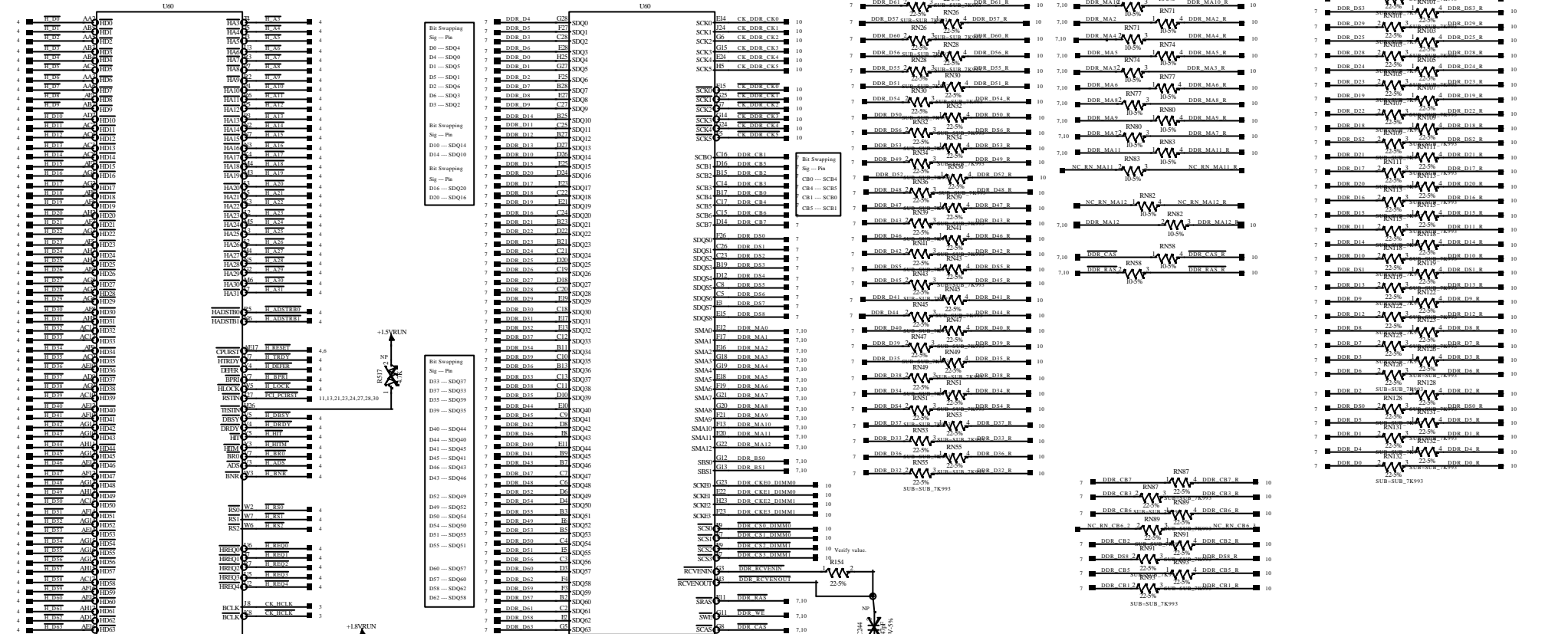
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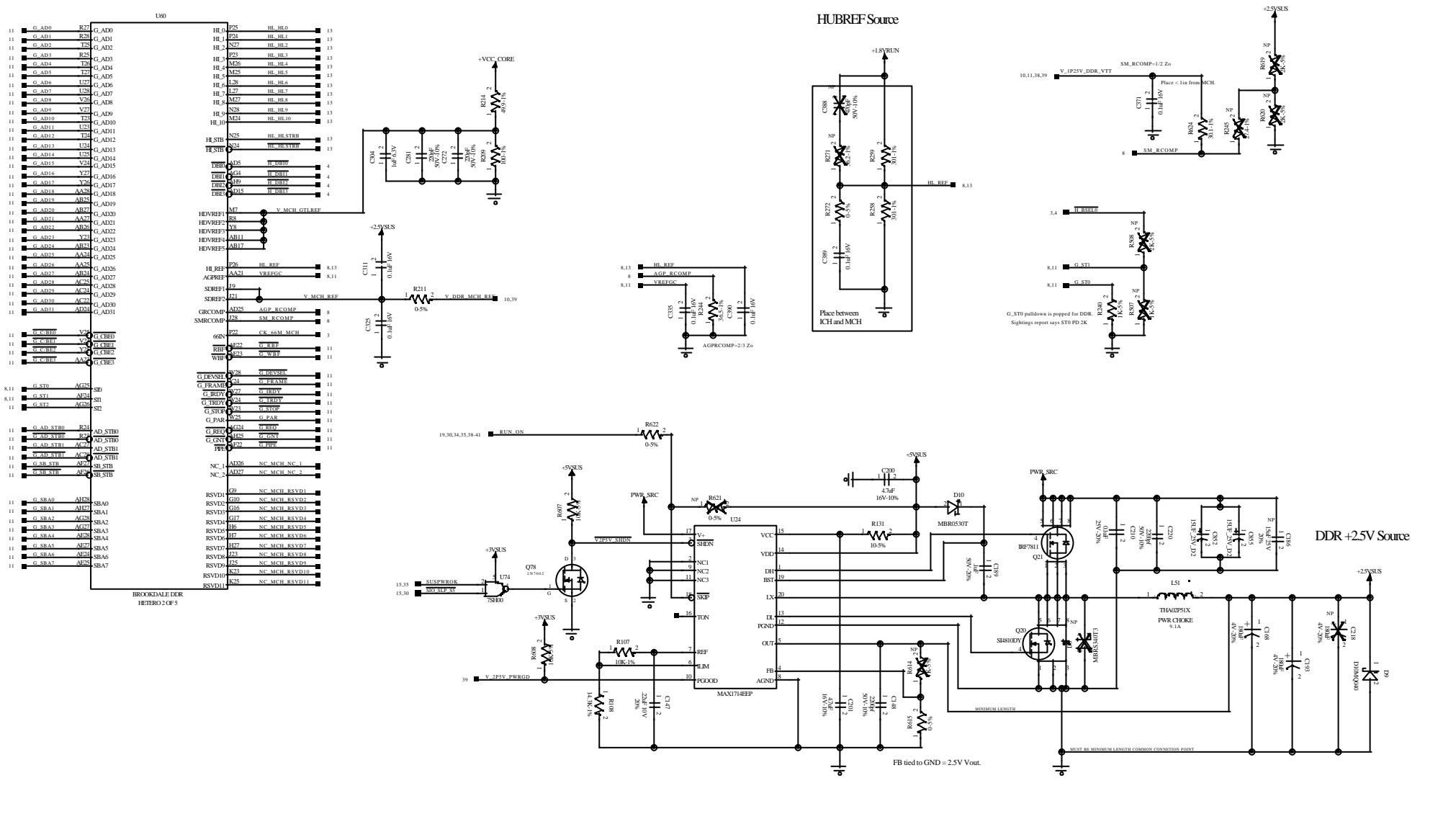
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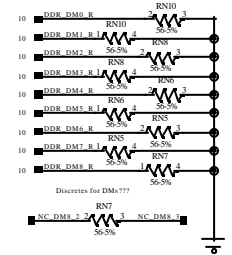
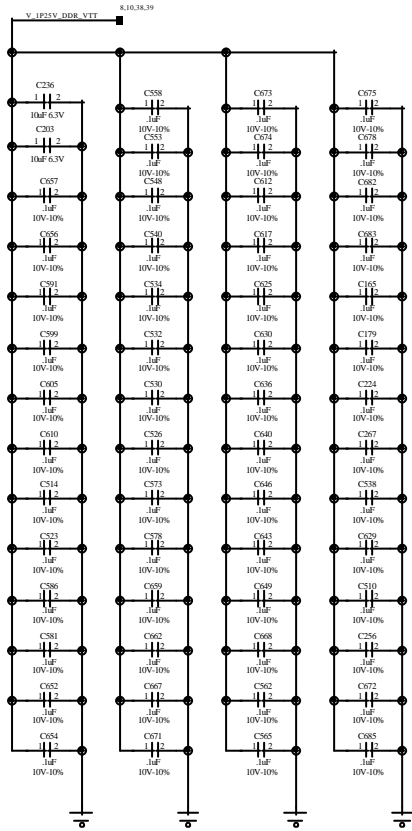
A

B

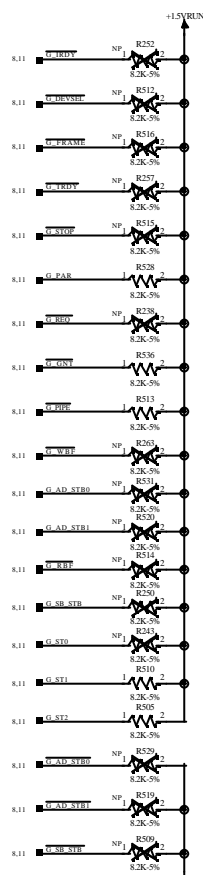
C

D

DDR VTT decoupling.

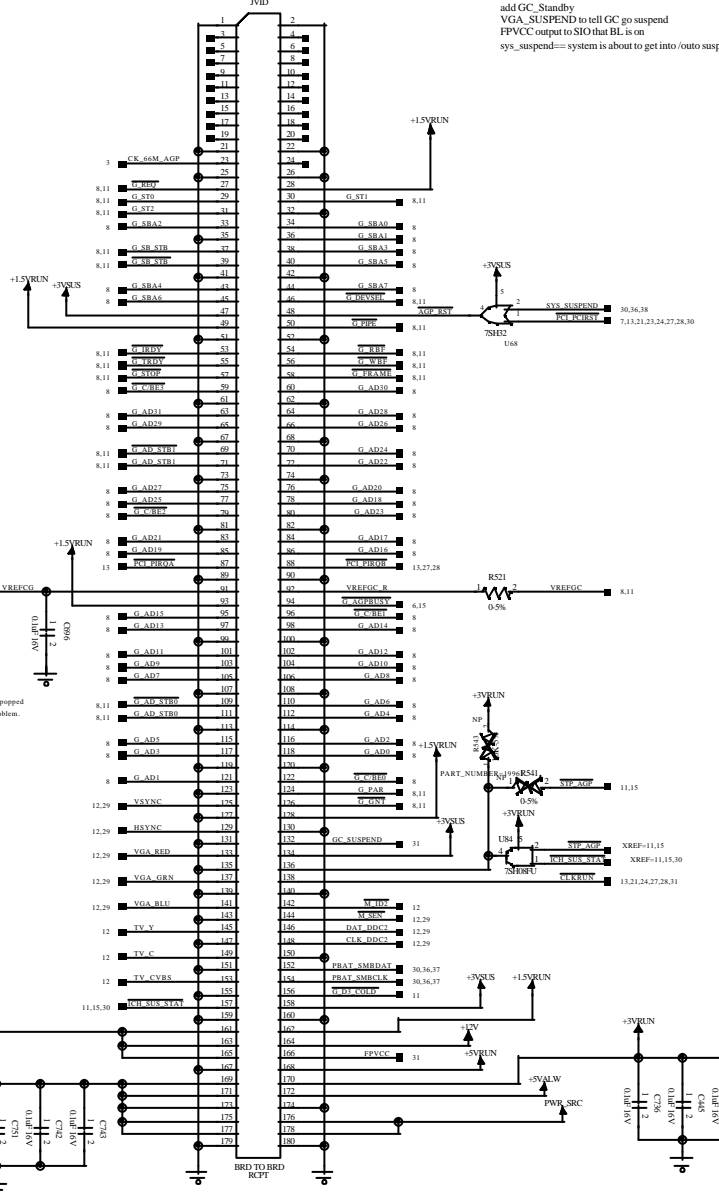


AGP pullups: matches Meteor. Verify pullups in Brookdale.

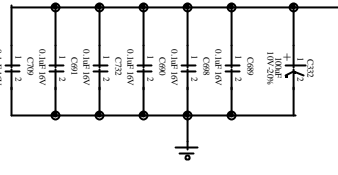


R953 and R498 are popped due to BD-M AD problem.

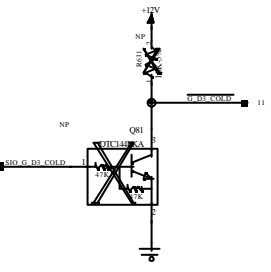
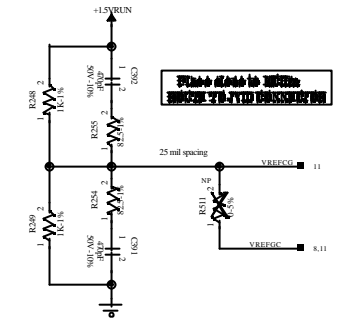
VGA Board Connector



vga-off==vga_suspend
 v_vga==comes from 3VSUS and 5vSus
 add GC_Suspend
 add GC_Standby
 VGA_SUSPEND to tell GC go suspend
 FPVCC output to SIO that BL is on
 sys_suspend== system is about to get into /outo suspend

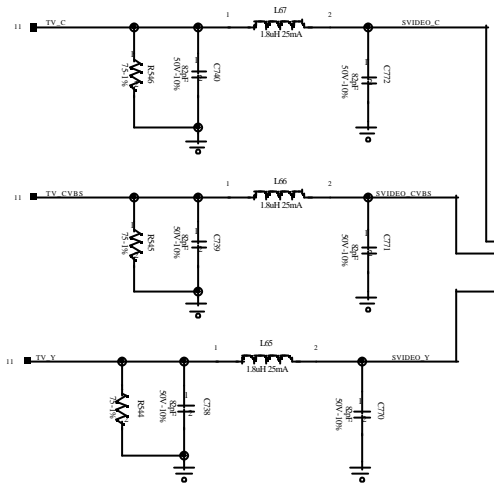


VREFCG Source

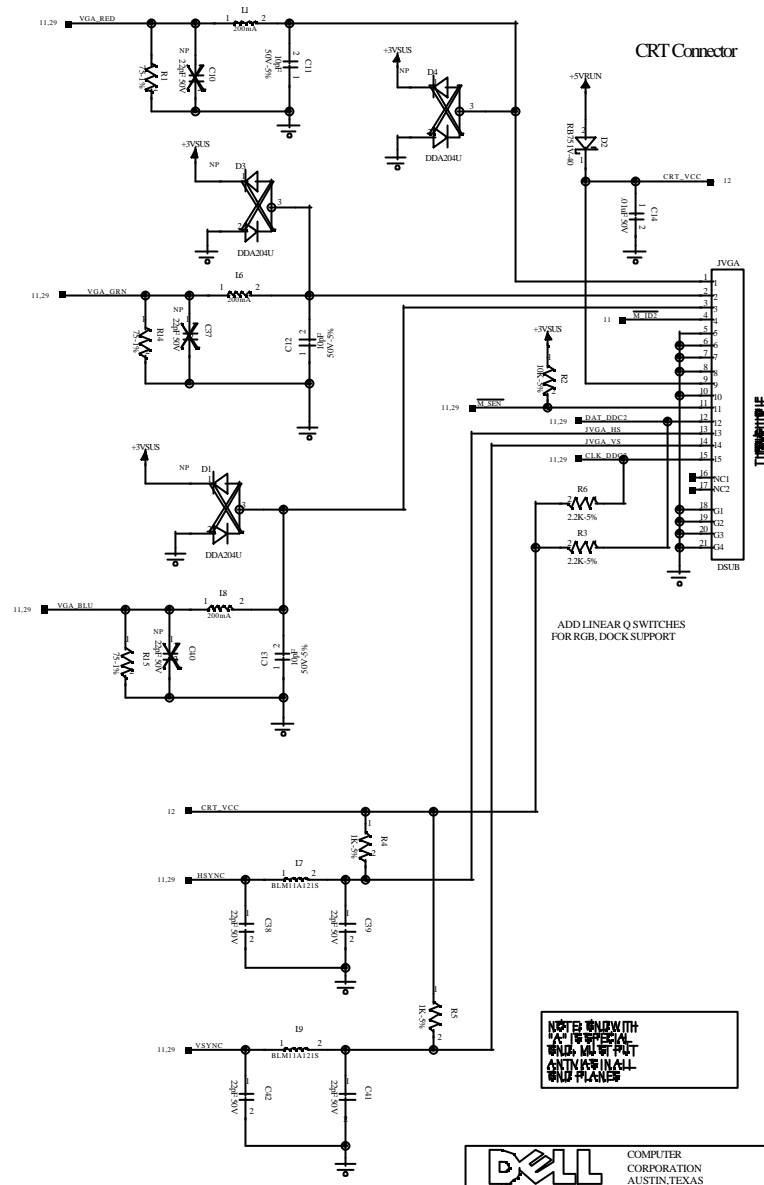
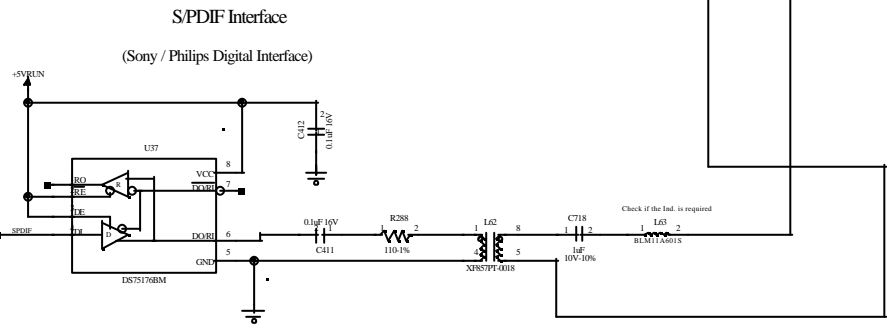
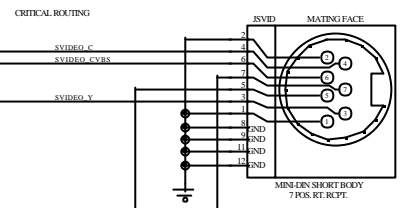


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S-Video Connector



DO NOT MIX WITH ANY OTHER PLANT AND WIRE IN ALL WIRE PLANES

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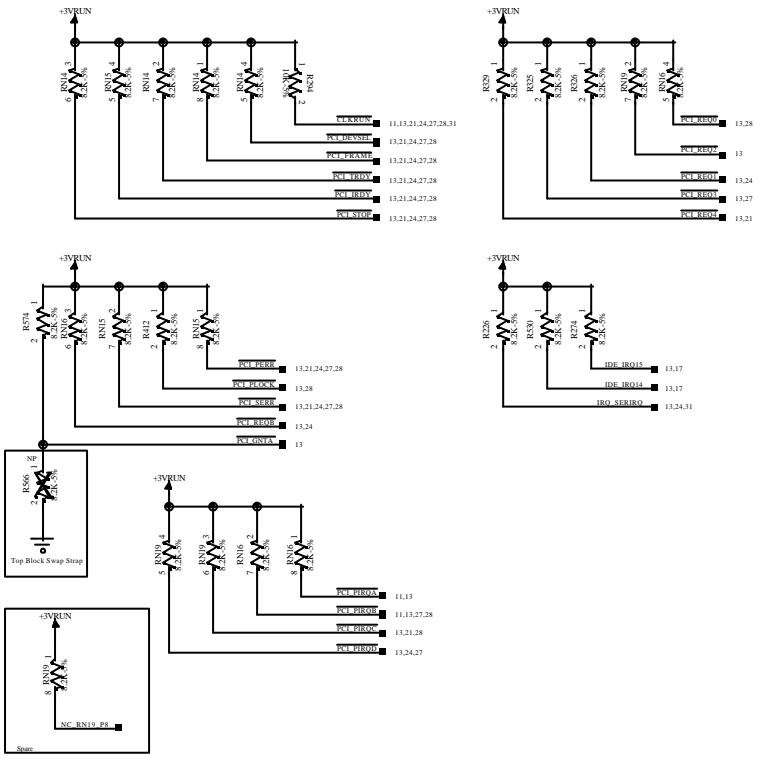
A

B

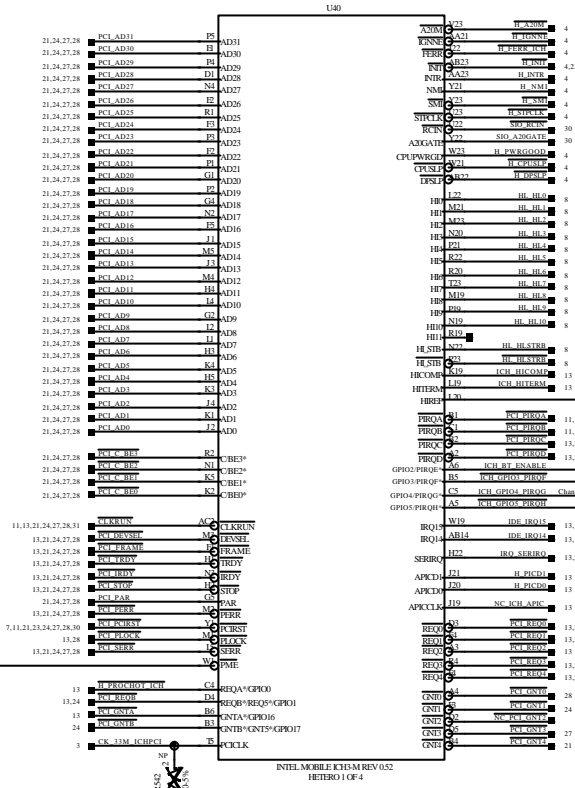
C

D

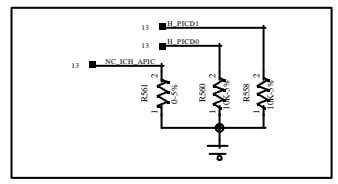
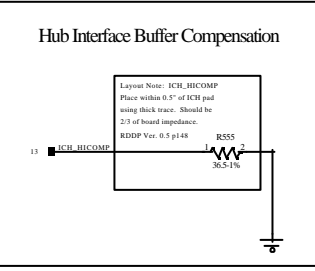
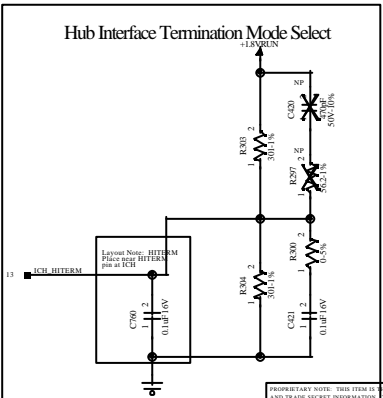
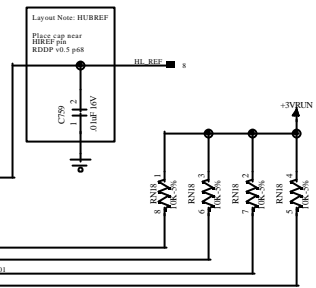
PCI Bus Pull-Ups



ICH3-M (1/4) PCI/CPU/Hublink Interface



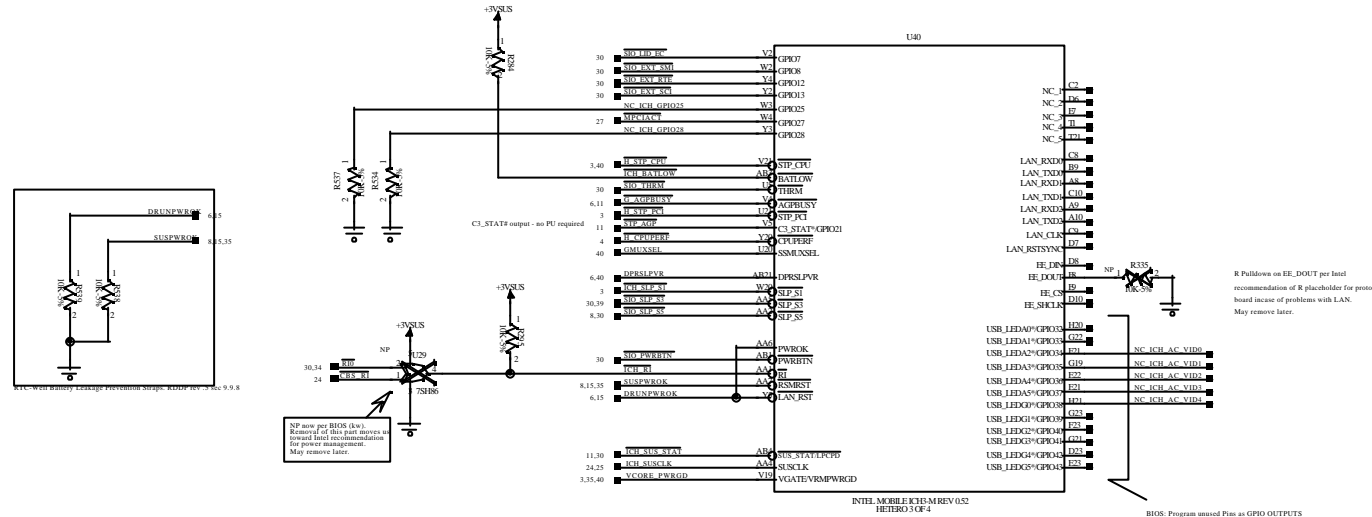
HUB INTERFACE LAYOUT:
ROUTE SIGNALS WITH 5:20 TRACE SPACE.
SIGNALS MUST MATCH +/-0.1" OF HL_STB*STB* SIGNALS.
RDDP Ver. 0.5 p148



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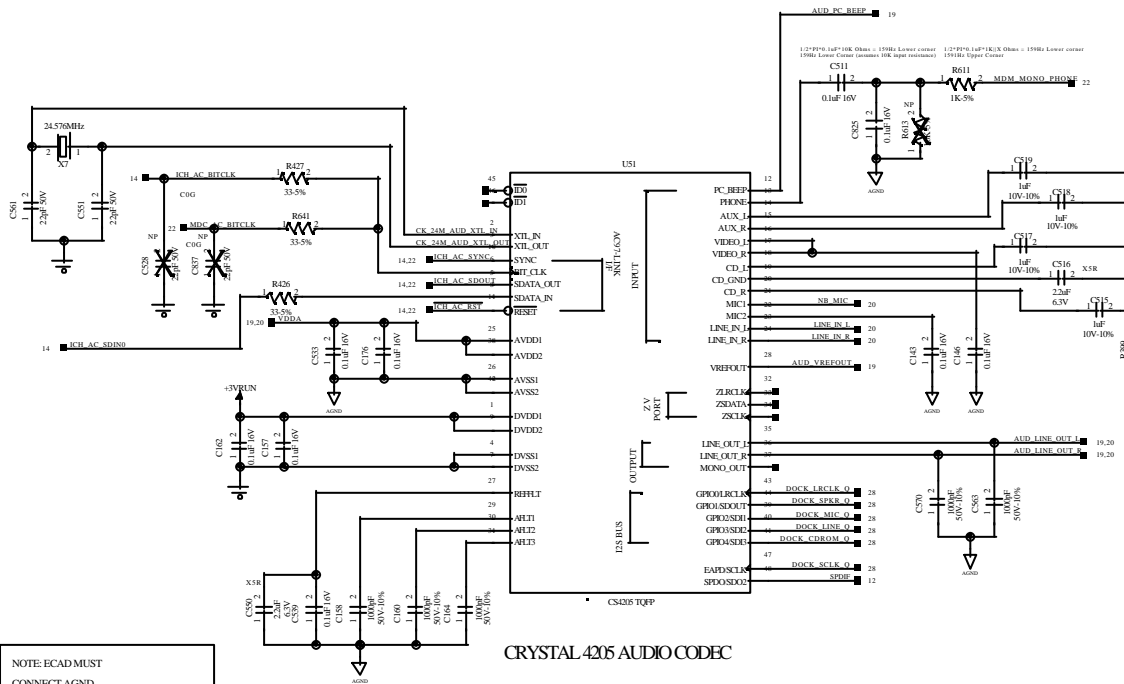
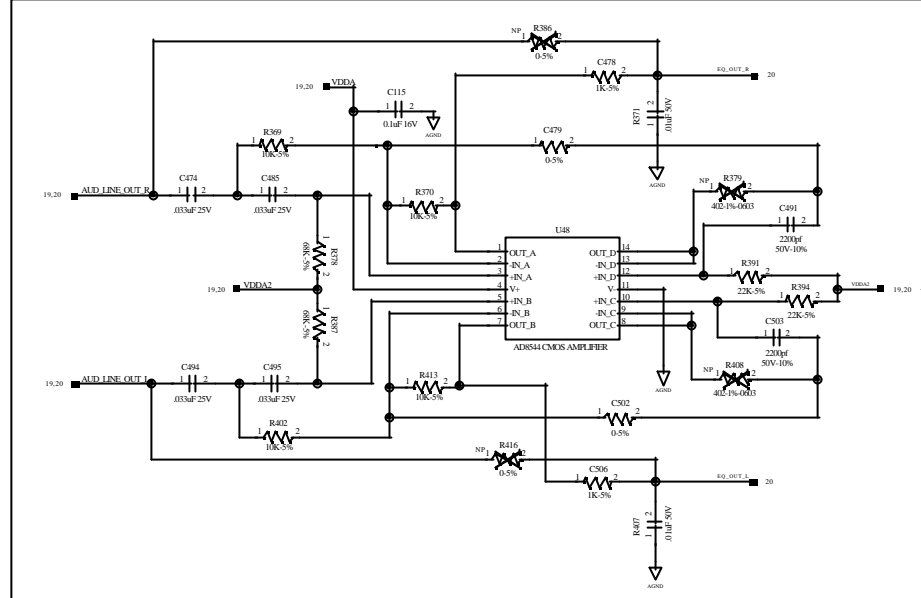
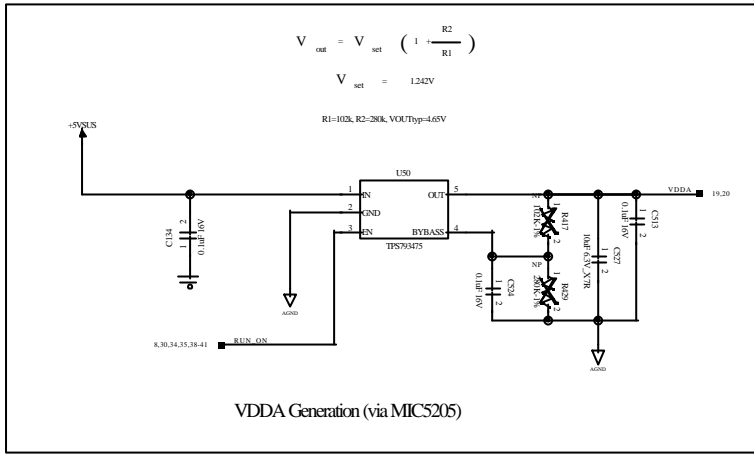
ICH3-M (3/4) PWR MGMT / LAN / USBLED Interface



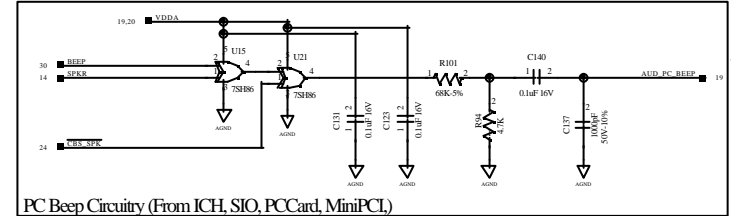
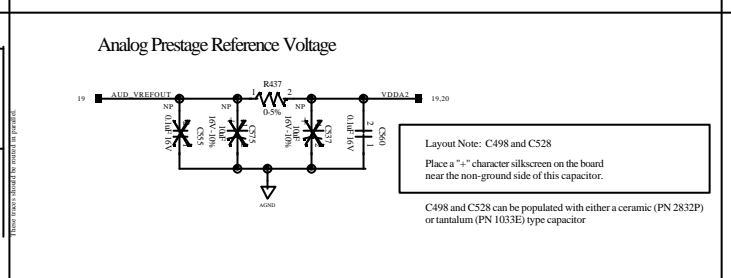
R Pulldown on EE_DOUT per Intel
recommendation of R placeholder for proto
board issue of problems with LAN.
May remove later.

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AND TRADE SECRET INFORMATION. THIS ITEM MAY NOT BE TRANSFERRED FROM THE CUSTODY OF DELL COMPUTER CORP. EXCEPT
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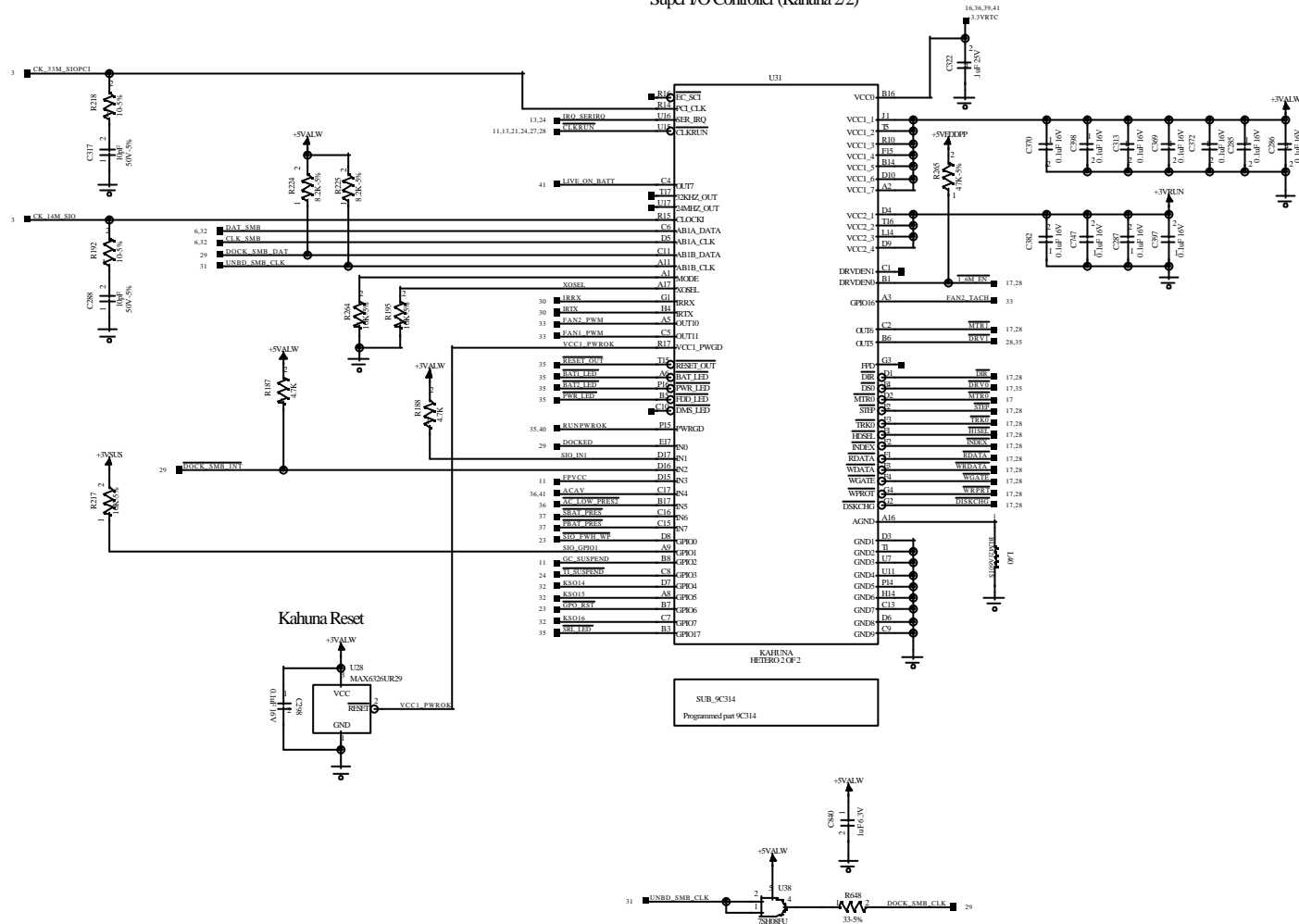
NOTE: ECAD MUST CONNECT AGND TO GND (VIA DRAWBRIDGE)!! 60 MIL TRACE AT ONE POINT ONLY UNDER THE CODEC



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Super I/O Controller (Kahuna 2/2)



Kahuna Reset

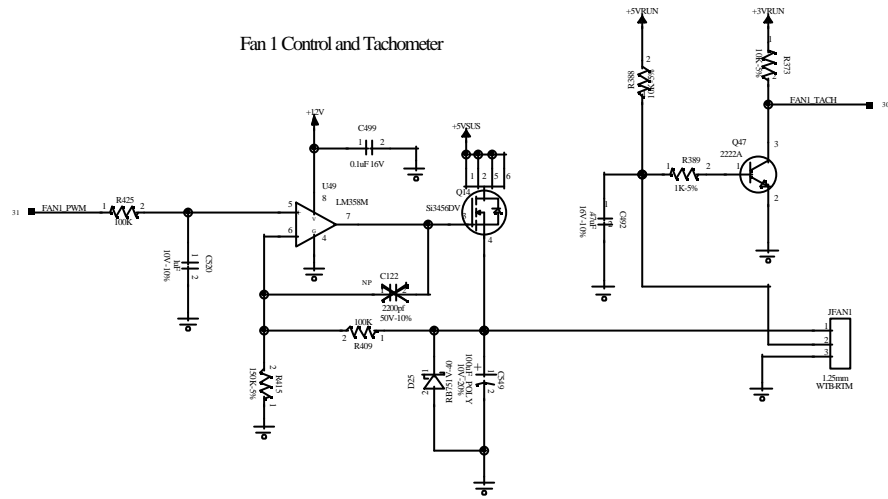
SUB_9C314
Programmed part 9C314

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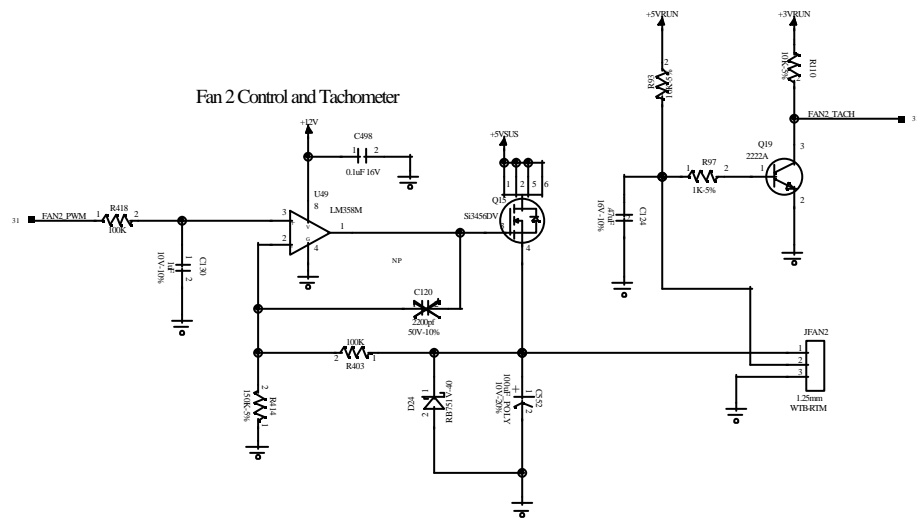
DELL		COMPUTER CORPORATION AUSTIN, TEXAS	
TITLE SCHEMATIC, M/B LA-1221			
DWG NO. 401195		REV. 4A	
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Fan Control Circuit

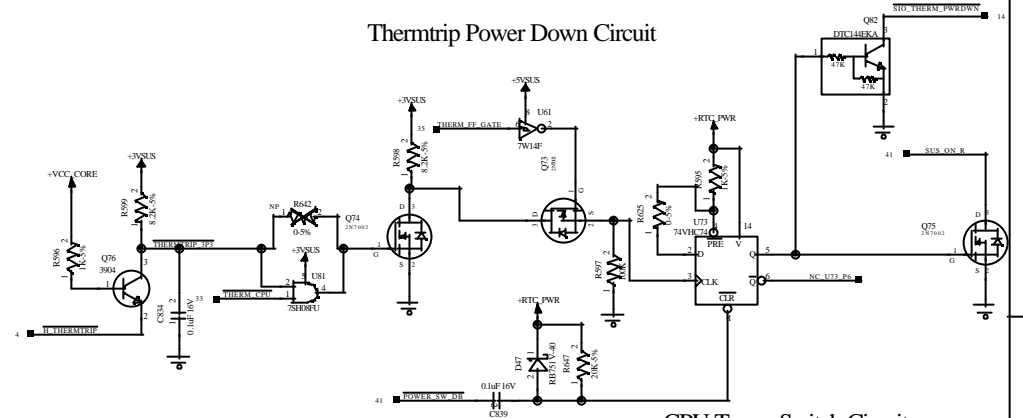
Fan 1 Control and Tachometer



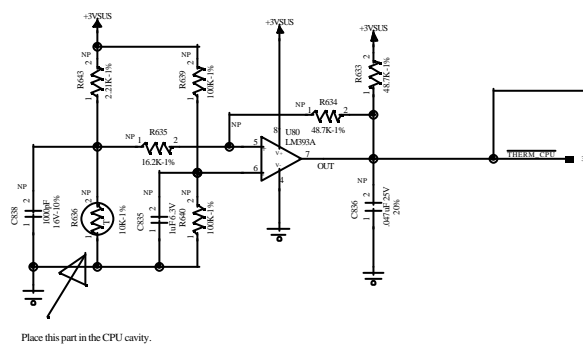
Fan 2 Control and Tachometer



Thermtrip Power Down Circuit

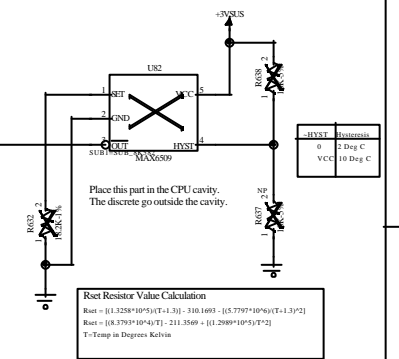


CPU Thermistor Circuit



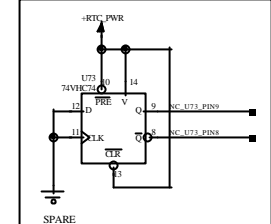
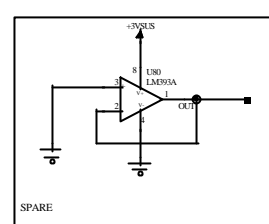
Place this part in the CPU cavity.

CPU Temp. Switch Circuit



Place this part in the CPU cavity.
The discrete go outside the cavity.

Resistor Value Calculation
 $R_{set} = (1.2258 \times 10^5) \times (T - T_0) - 310.1493 - (5.7797 \times 10^6) \times (T - T_0)^2$
 $R_{set} = (8.3793 \times 10^4) \times (T) - 211.3569 - (1.2989 \times 10^5) \times (T^2)$
 T = Temp in Degrees Kelvin



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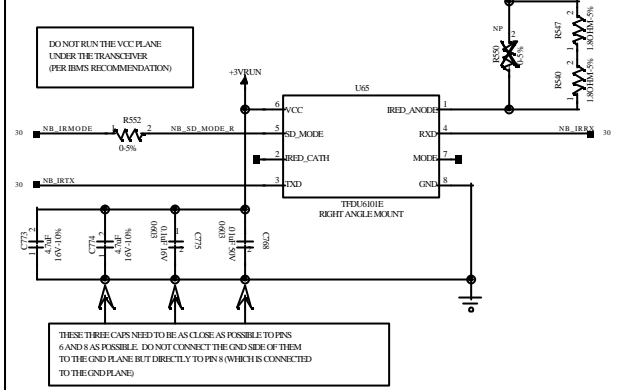
A

B

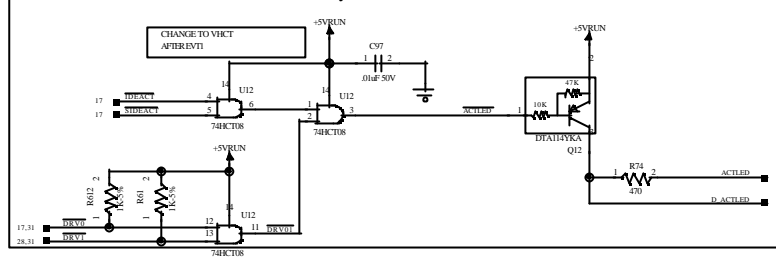
C

D

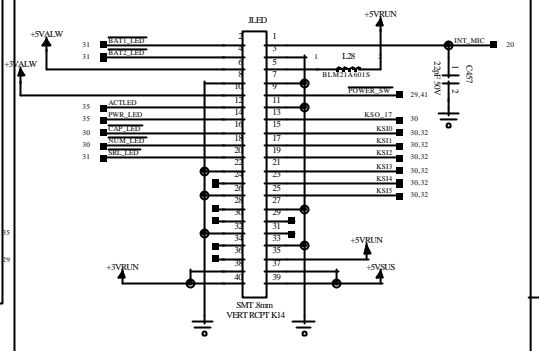
On-board IR Transceiver



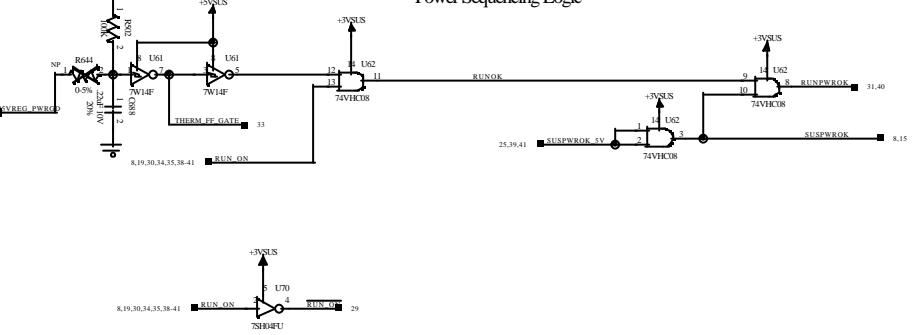
Activity LED Driver for Internal Drives



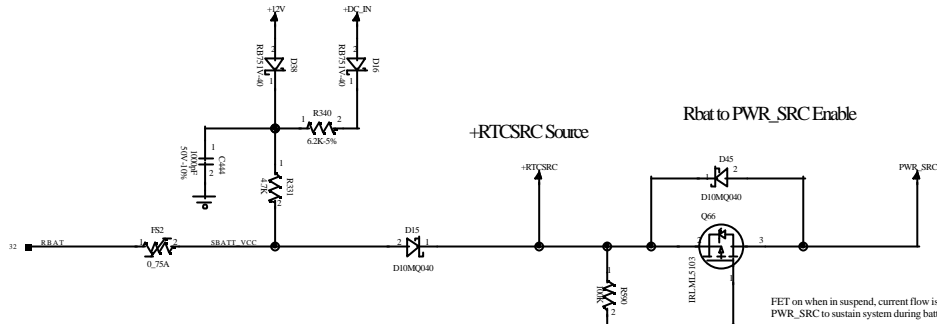
LED Board Connector



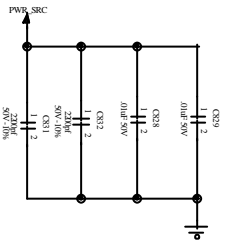
Power Sequencing Logic



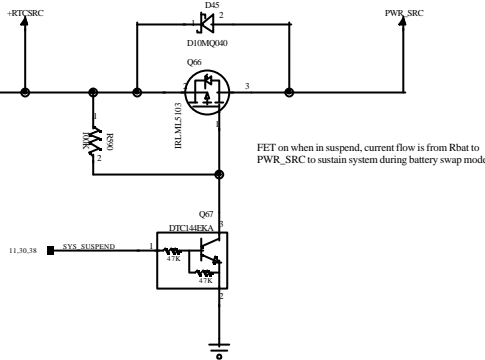
Rbat Charger



USE MULTIPLE VIAS FOR TRANSIENS

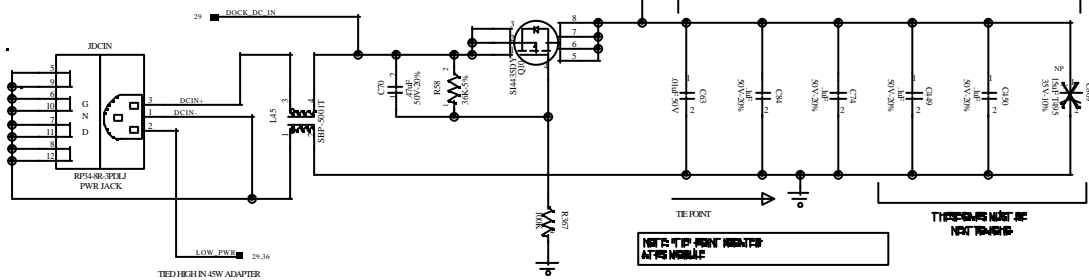


Rbat to PWR_SRC Enable

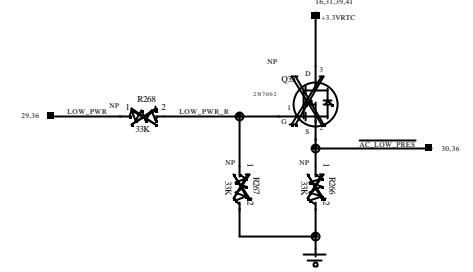


SAFETY WARNING
FOR REMOVAL OF THE FUSE

AC Adaptor Connector

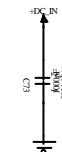
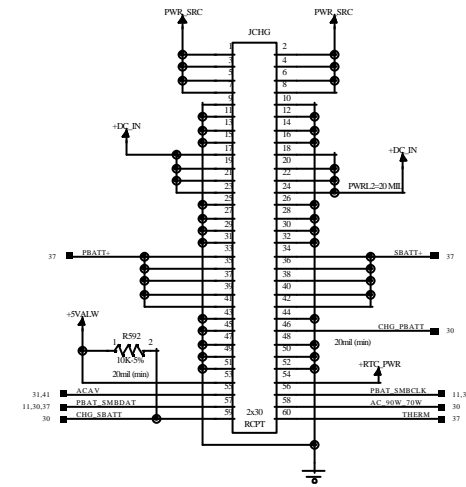


Low-Power Adapter Detection



LOW_PWR	AC_LOW_PRES#	AC_LOW_PRESM
0V	0	0
FLOAT	0	1
20V	1	1

Charger Board Connector



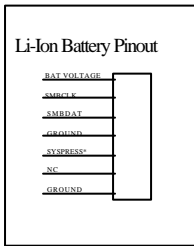
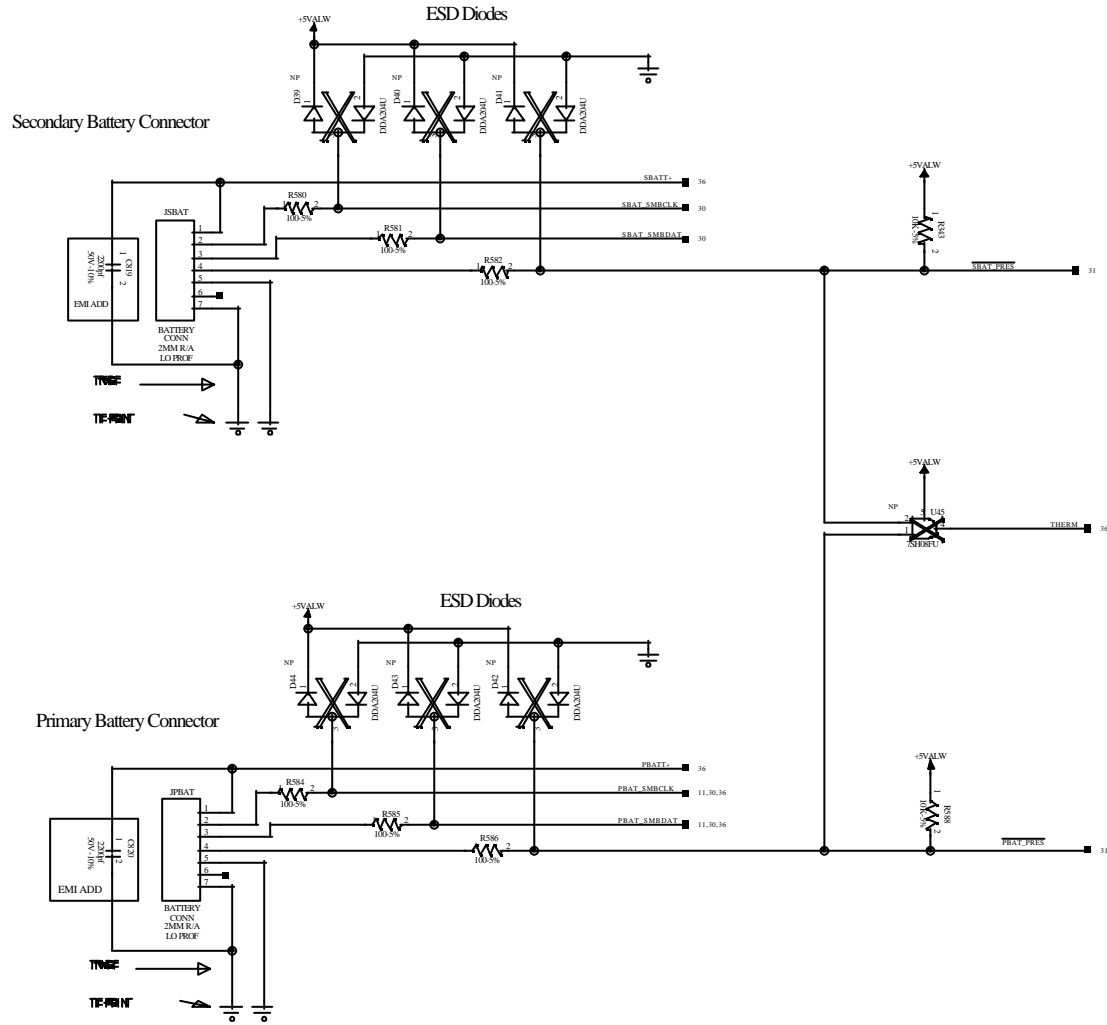
DELL COMPUTER CORPORATION AUSTIN, TEXAS

TITLE: SCHEMATIC, M/B LA-1221

PWG NO: 401195 REV: 401195

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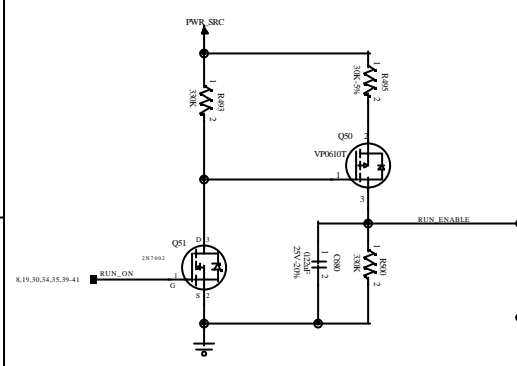
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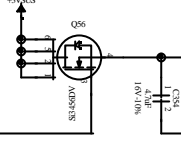
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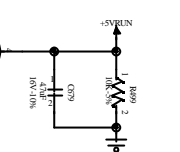
Run Planes Enable



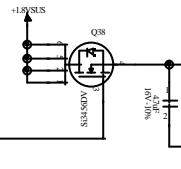
+3VRUN Source



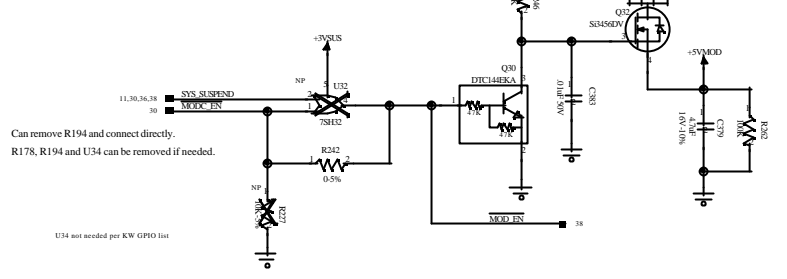
+5VRUN Source



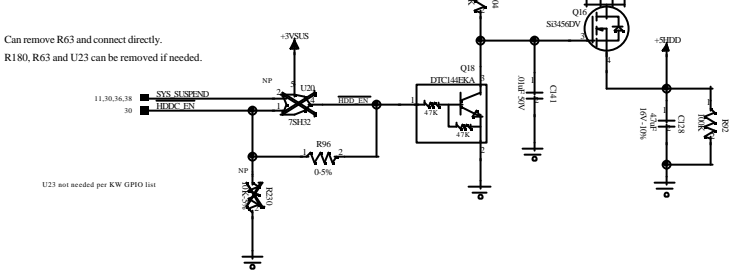
+1.8VRUN Source



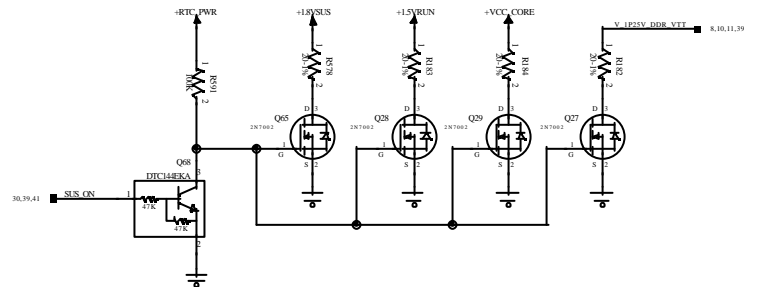
+5VMOD Source



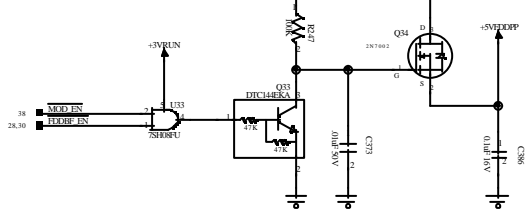
+5HDD Source



Voltage Rail Drains

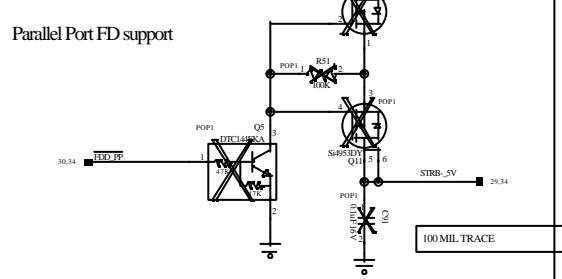


+5VFDDPP Source



REMOVE THIS

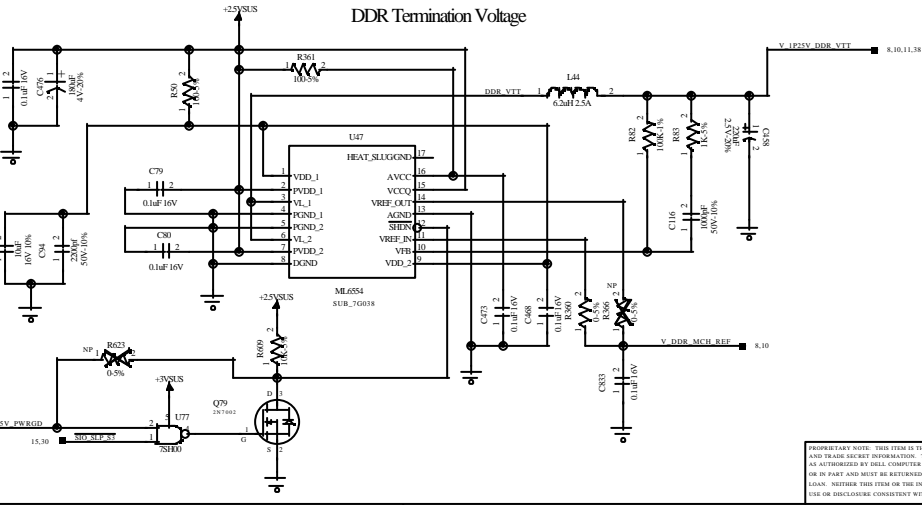
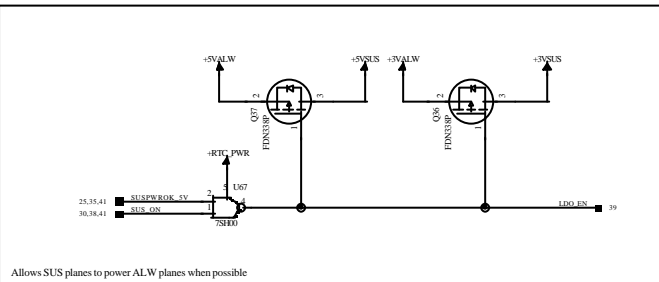
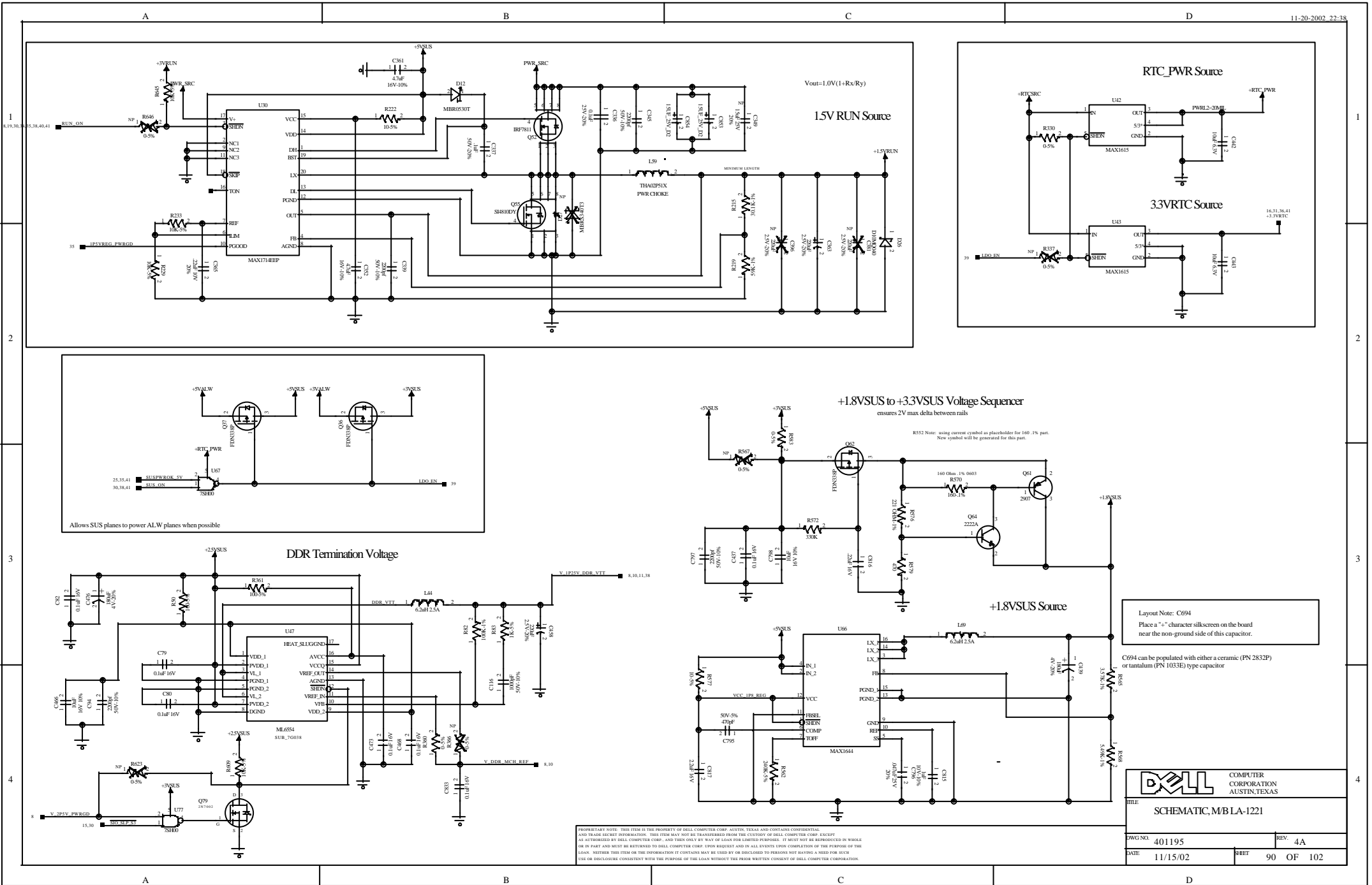
STRB_5V Source



Parallel Port FD support

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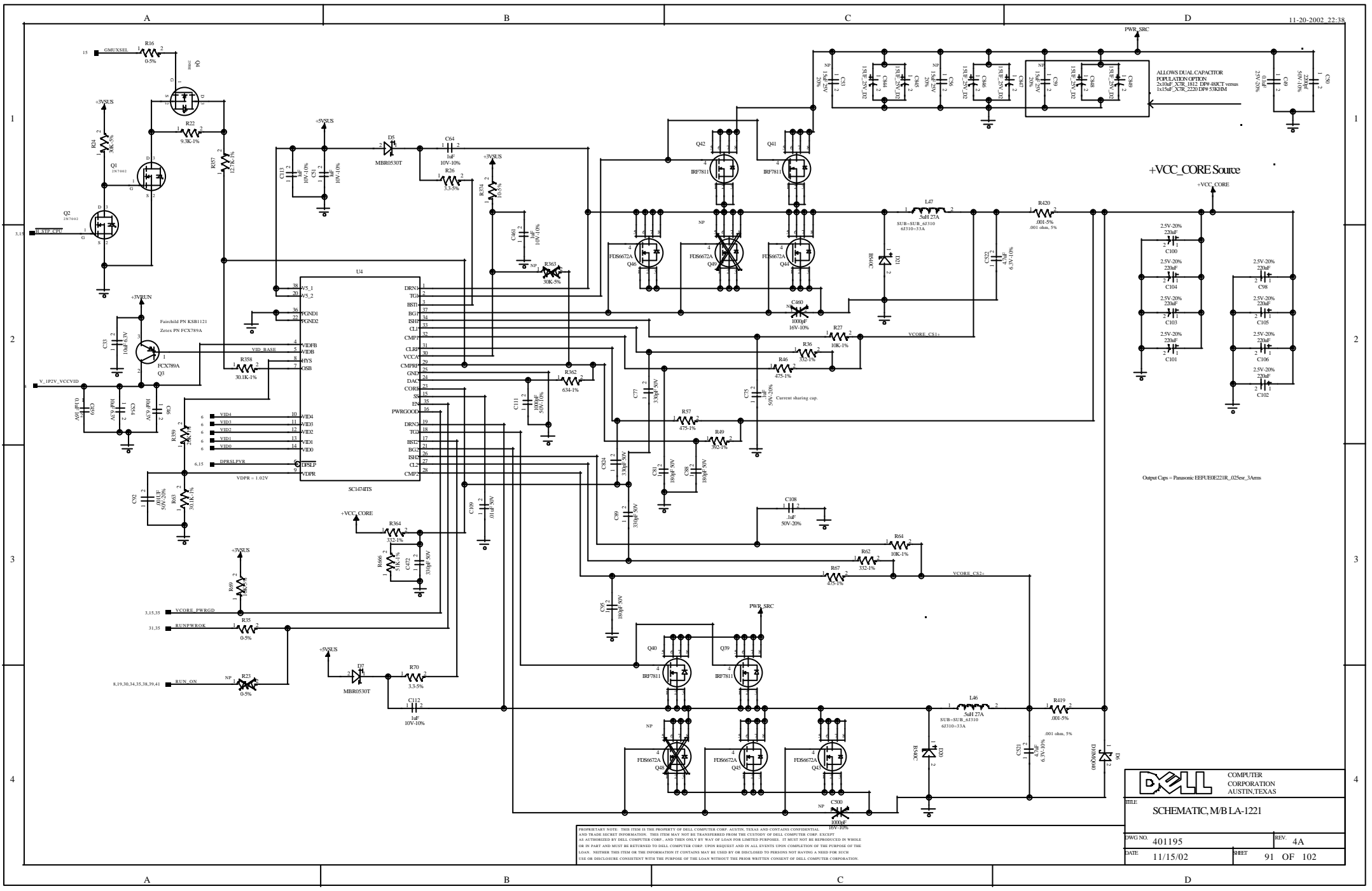
DELL		COMPUTER CORPORATION AUSTIN, TEXAS	
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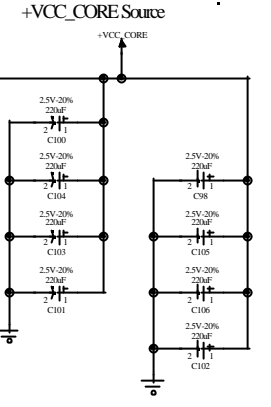
Layout Note: C694
Place a "+" character silkscreen on the board near the non-ground side of this capacitor.

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ALLOWED DUAL CAPACITOR POPULATION OPTION
 2x10µF XCR 1812 EPO 85CCT versus
 1x10µF XCR 2221 EPO 85CCTM

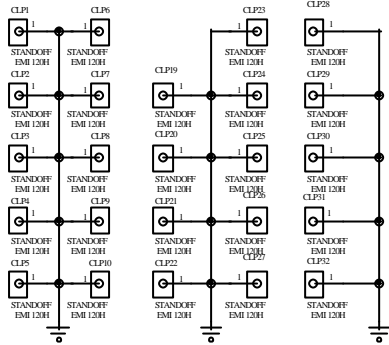


Output Caps = Parasonic EEFUEE221R_02Ser_3Amm

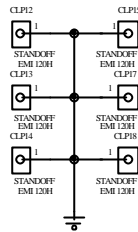
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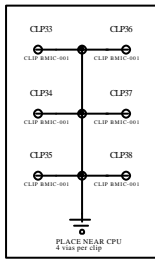
Memory Door EMI Clips



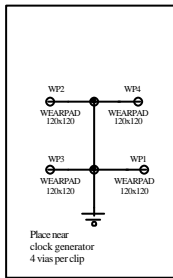
Mini-PCI Door EMI Clips



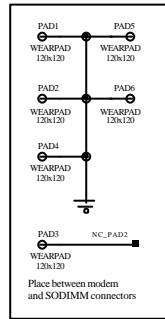
CPU EMI Clips



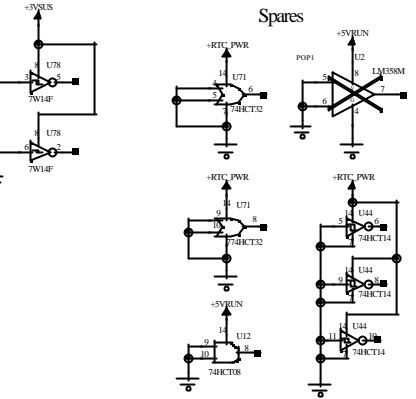
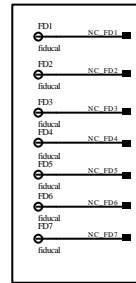
Clock Generator EMI Clips



Modem Fence Pads



Fiducial mark



1

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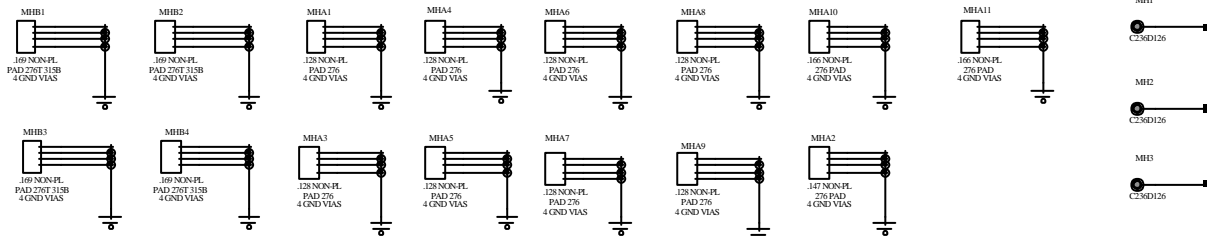
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Mounting Holes



Xibom requires ADD attributes to be attached to an instance of a symbol (prefix I in the wire file). You may "nop" rename the attributes. The required order is: ADD, ADD1, ADD2, ...

ADD=ADD_3F195_PWB
 ADD1=ADD_1F475_SCHISM
 ADD2=ADD_0F481_ASSYDVG
 ADD3=ADD_42753_BARCODE_REVLEVEL
 ADD4=ADD_12410_BARCODE_IDLABEL Label: LBL_ID, BARCODE.PWA
 PWA 2F219

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A

B

C

D

A

B

C

D

Schematic Change List

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4

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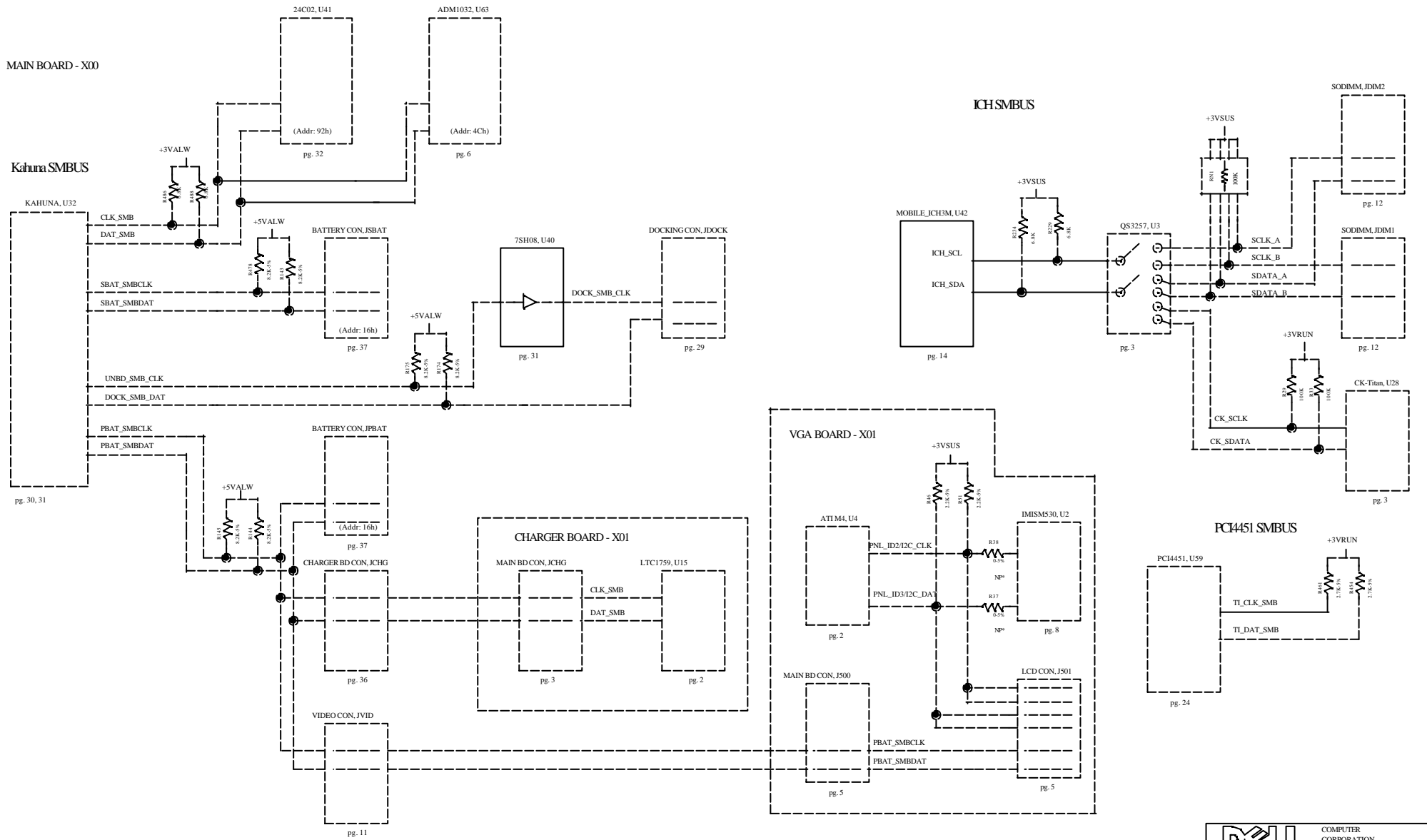
D

MAIN BOARD - X00

Kahuna SMBUS

ICH SMBUS

PCI4451 SMBUS



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