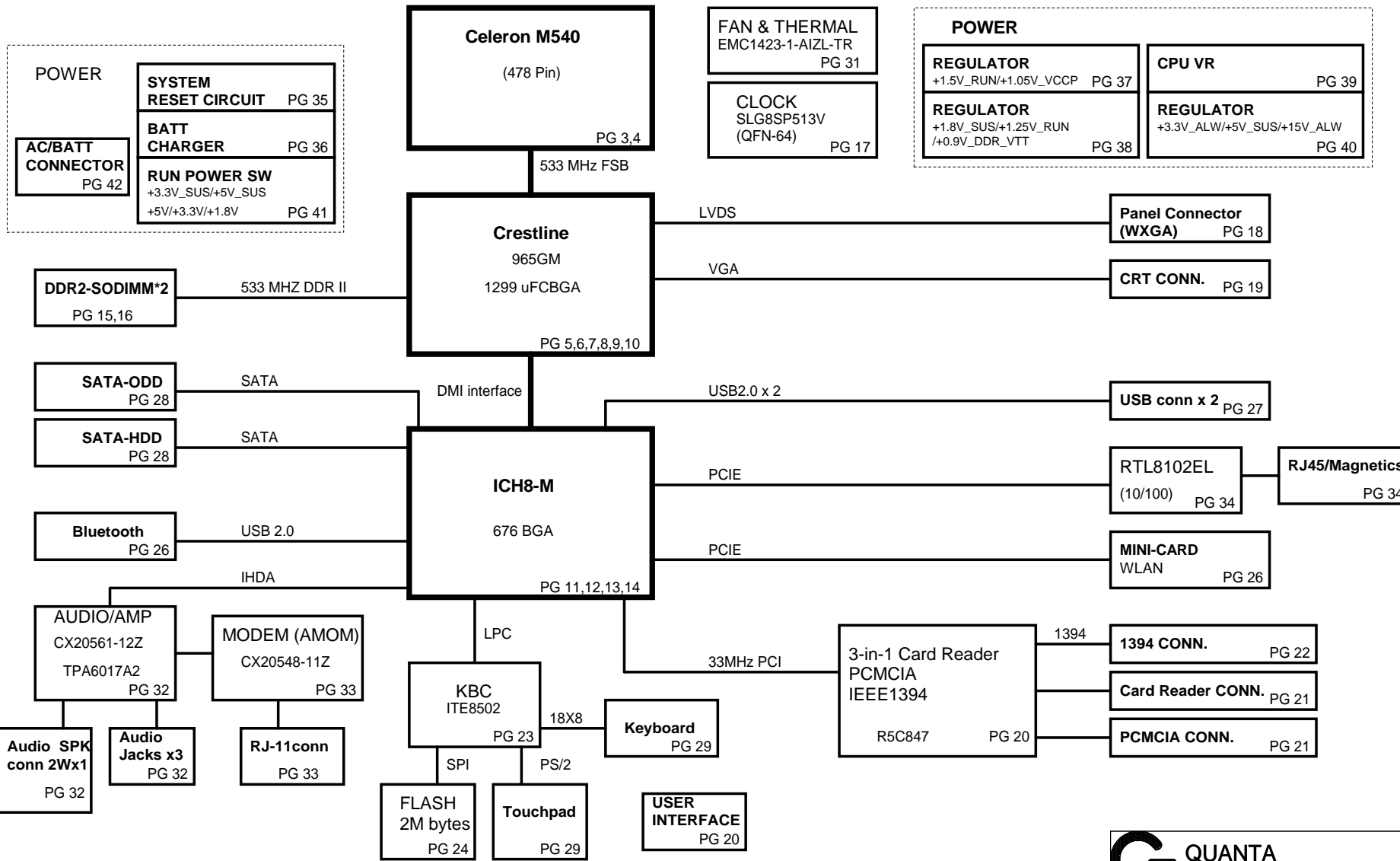


# VM9/VM8 Block Diagram

VER : 1A



Title			Schematic Block Diagram		
Size	Document Number	Rev			
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PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
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15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	HDMI
23	LCD Conn. & SSP
24	CRT Conn
25	SATA Conn
26-27	CARD READER/Conn & 1394
28	Express Card & Smart Card
29-30	Mini Card
31	SIO (ITE8512)
32	FLASH/RTC
33	USB
35	TP / KEYBOARD
36	SWITCH /LED
37	FAN & Thermal
38-39	Audio CODEC(ALC888)/Phone Jack
40-41	LOM / Switch
44	System Reset Circuit
46	Battery Selector & Charger
48	1.05VCCP / 1.5VRUJN
49	DDR2_1.8VSUS, 0.9V
51	CPU_ISL6266(2phase)
52	MAX8744 (+5.5V,+3.3V)
53	RUN Power Switch
54	DCIN,Batt
55	PAD& SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Dianram

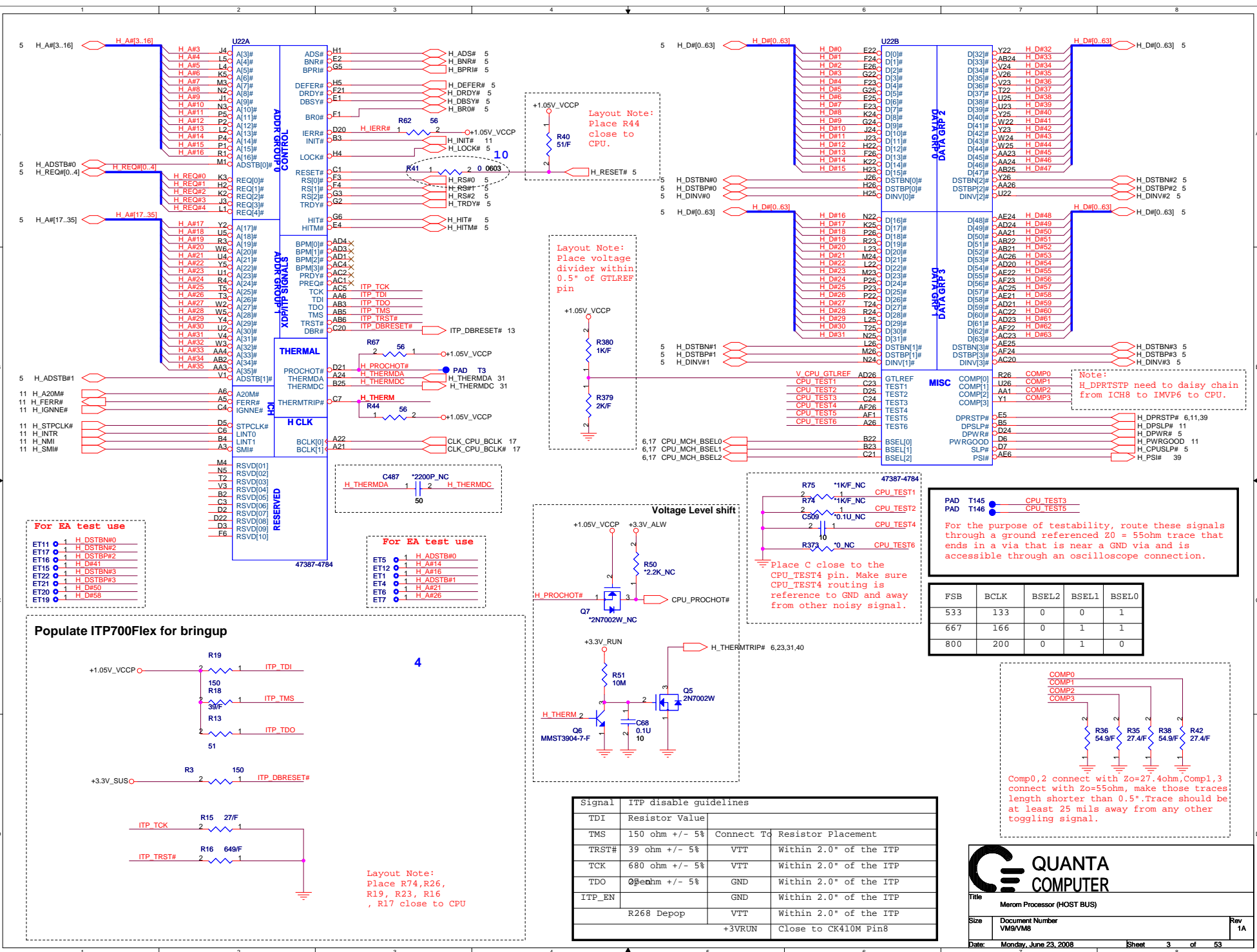
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54,56	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	18,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDCC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

GND PLANE	PAGE	DESCRIPTION
⏚ 8731AGND	46	
⏚ AGND_0.9V	49	
⏚ AGND_DC/DC	52	
⏚ AGND_DC2	48	
⏚ AGND_DDR	49	
⏚ AGND_ISL6260	51	
⏚ GND	ALL	

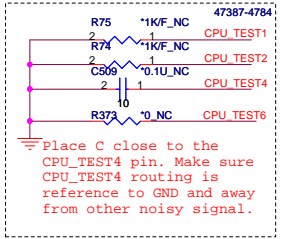
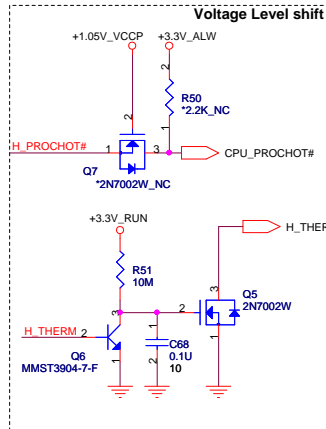
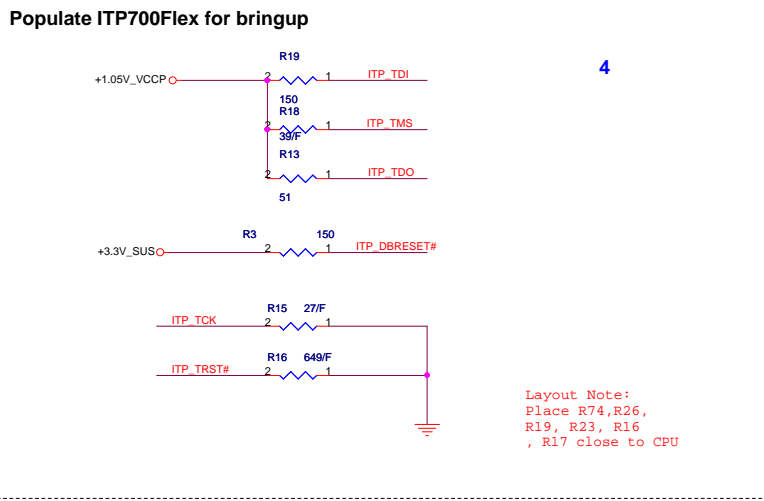


Title Index & Power Status		
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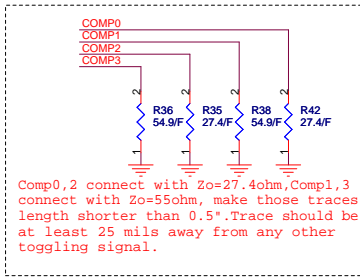
- For EA test use**
- ET11 1 H\_DSTBN#0
  - ET17 1 H\_DSTBP#2
  - ET16 1 H\_D#41
  - ET22 1 H\_DSTBN#3
  - ET21 1 H\_DSTBP#3
  - ET20 1 H\_D#50
  - ET19 1 H\_D#58

- For EA test use**
- ET5 1 H\_ADSTB#0
  - ET12 1 H\_A#14
  - ET1 1 H\_A#16
  - ET4 1 H\_ADSTB#1
  - ET6 1 H\_A#21
  - ET7 1 H\_A#26



For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



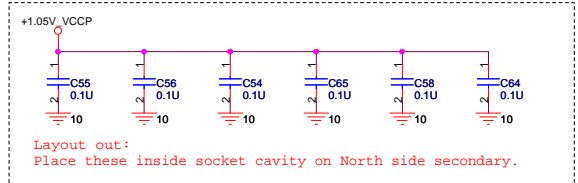
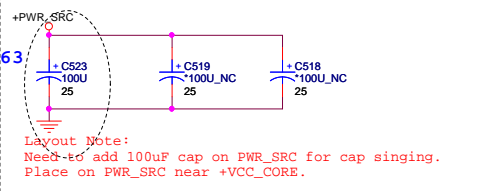
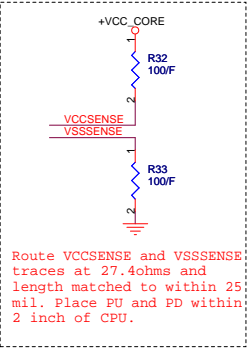
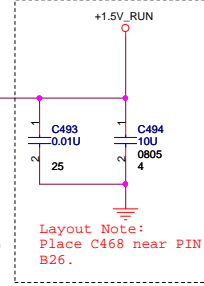
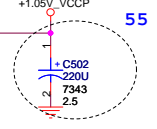
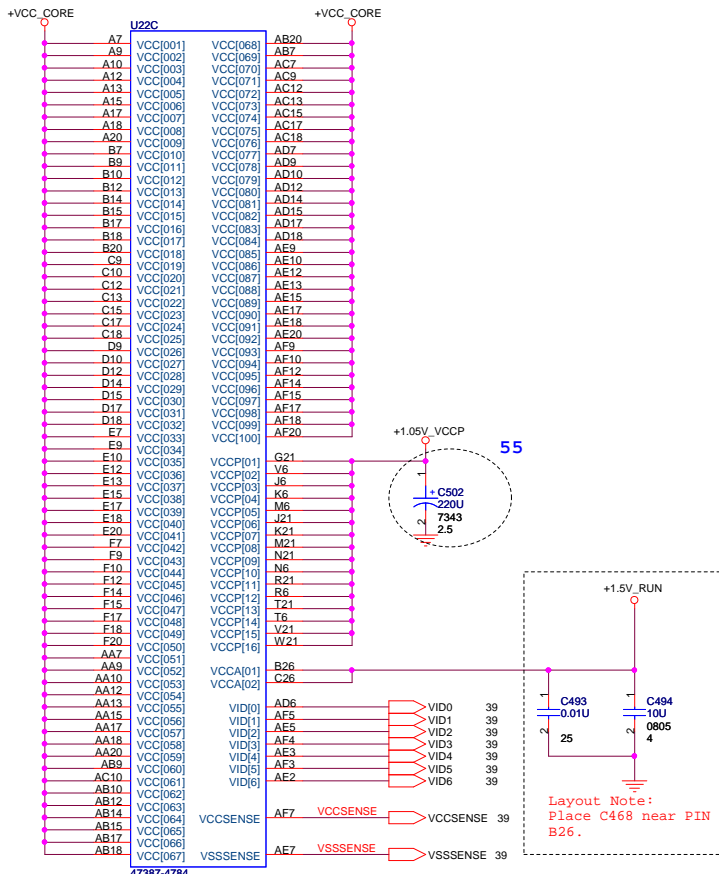
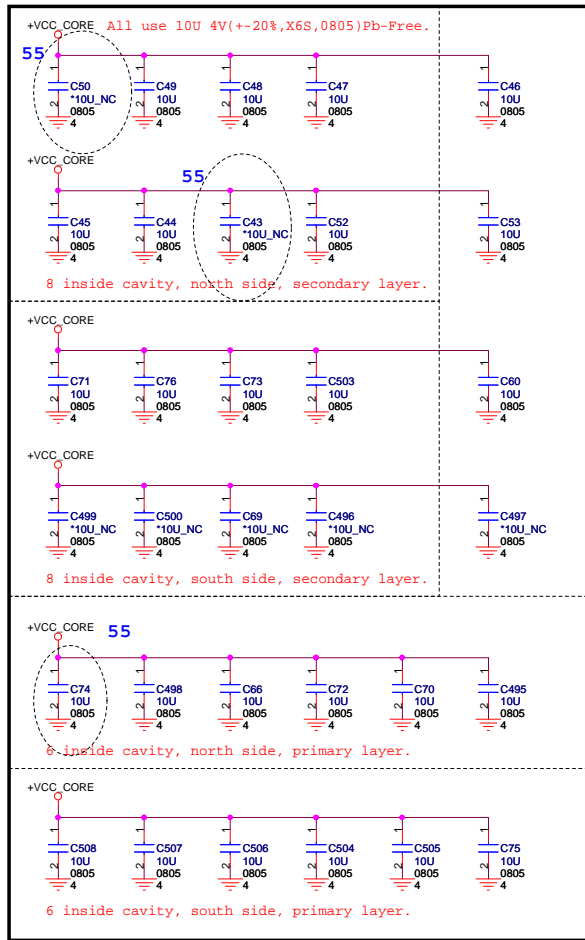
Signal	ITP disable guidelines		
TDI	Resistor Value	Connect To	Resistor Placement
TMS	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	0@enhm +/- 5%	GND	Within 2.0" of the ITP
ITP_EN	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

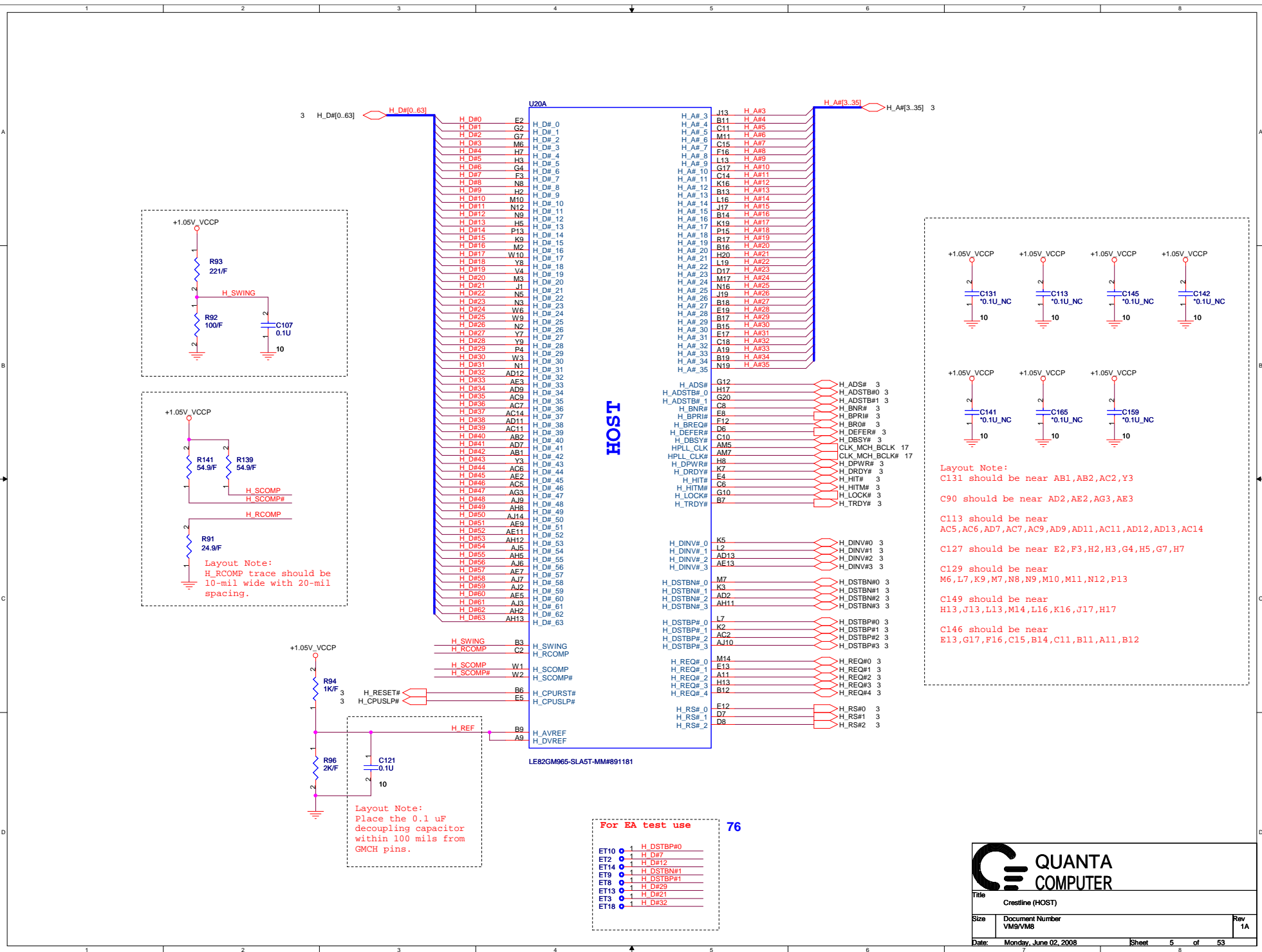
**QUANTA COMPUTER**

Title: Merom Processor (HOST BUS)

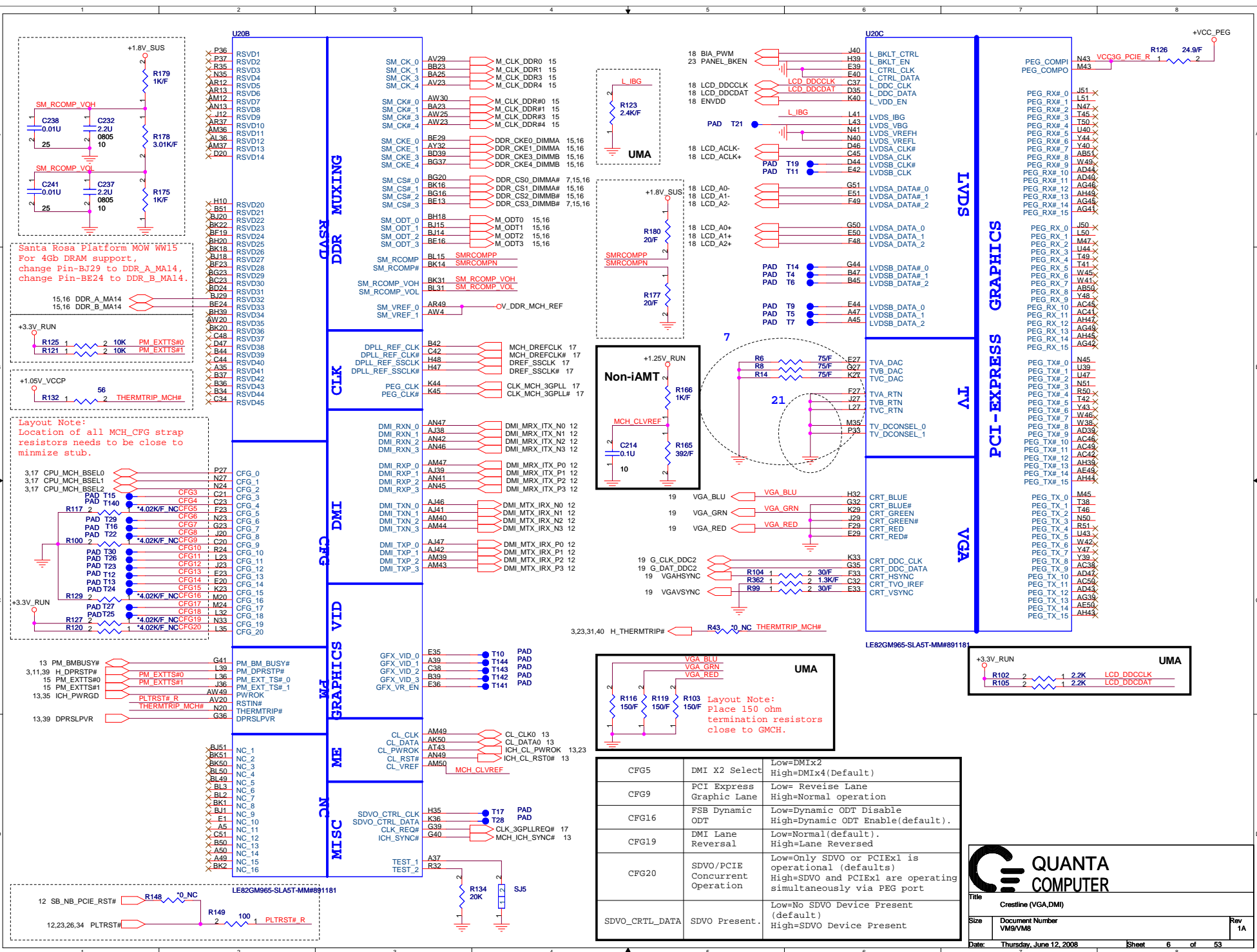
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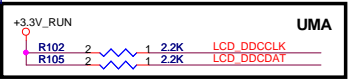
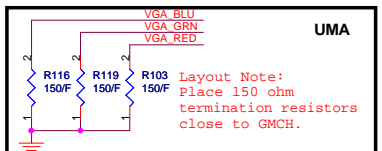
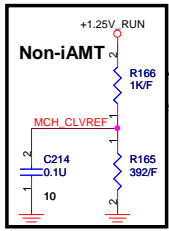


Title		Crestline (HOST)
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Santa Rosa Platform M0W Wv15  
For 4Gb DRAM support,  
change Pin-BJ29 to DDR\_A\_Ma14,  
change Pin-BE24 to DDR\_B\_Ma14.

Layout Note:  
Location of all MCH\_CFG strap  
resistors needs to be close to  
minimize stub.



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present..	Low=No SDVO Device Present (default) High=SDVO Device Present

**QUANTA COMPUTER**

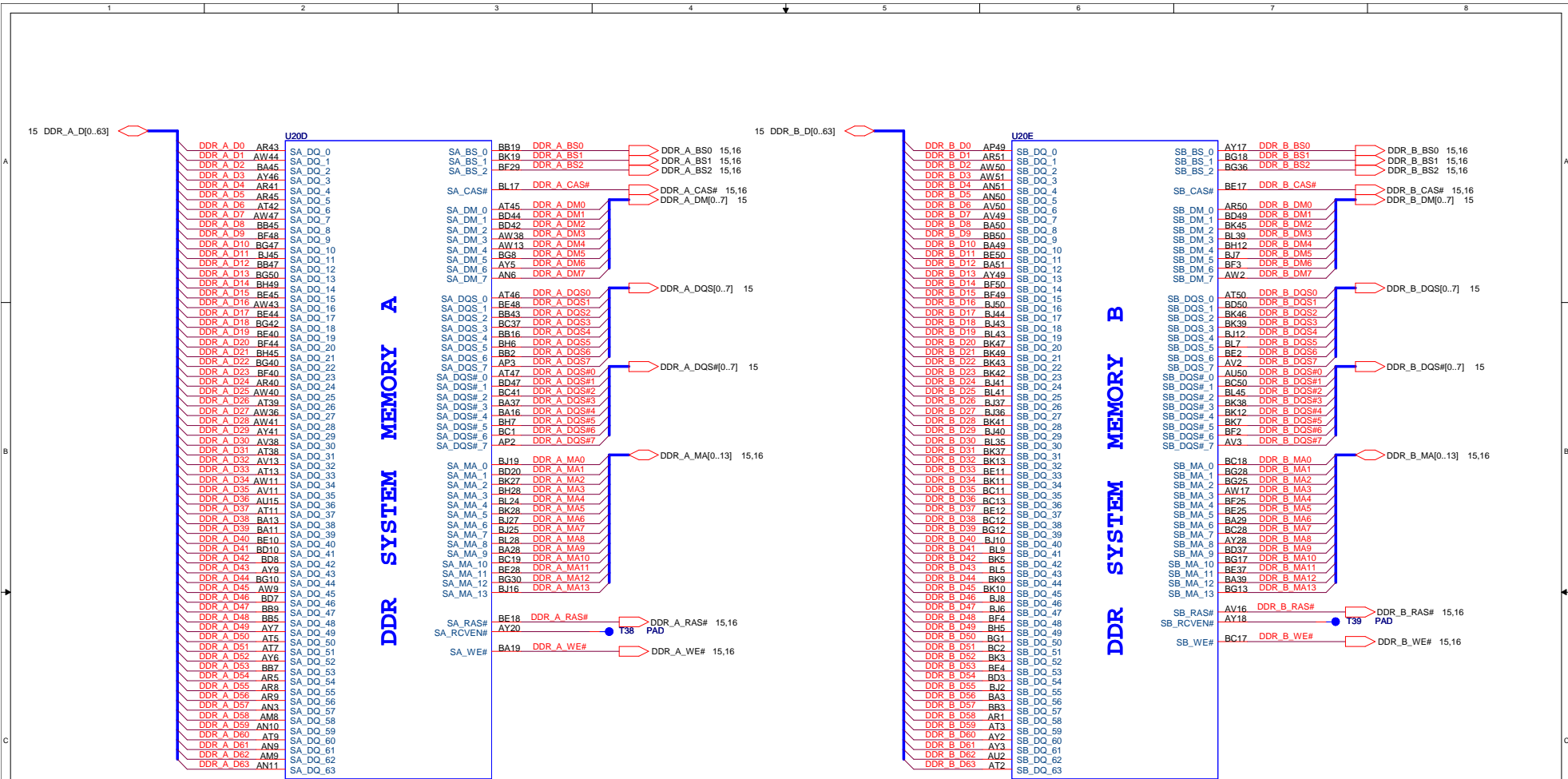
Title: Crestline (VGA,DMI)

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LE82GM965-SLA5T-MM#891181

LE82GM965-SLA5T-MM#891181

76: For EA test use

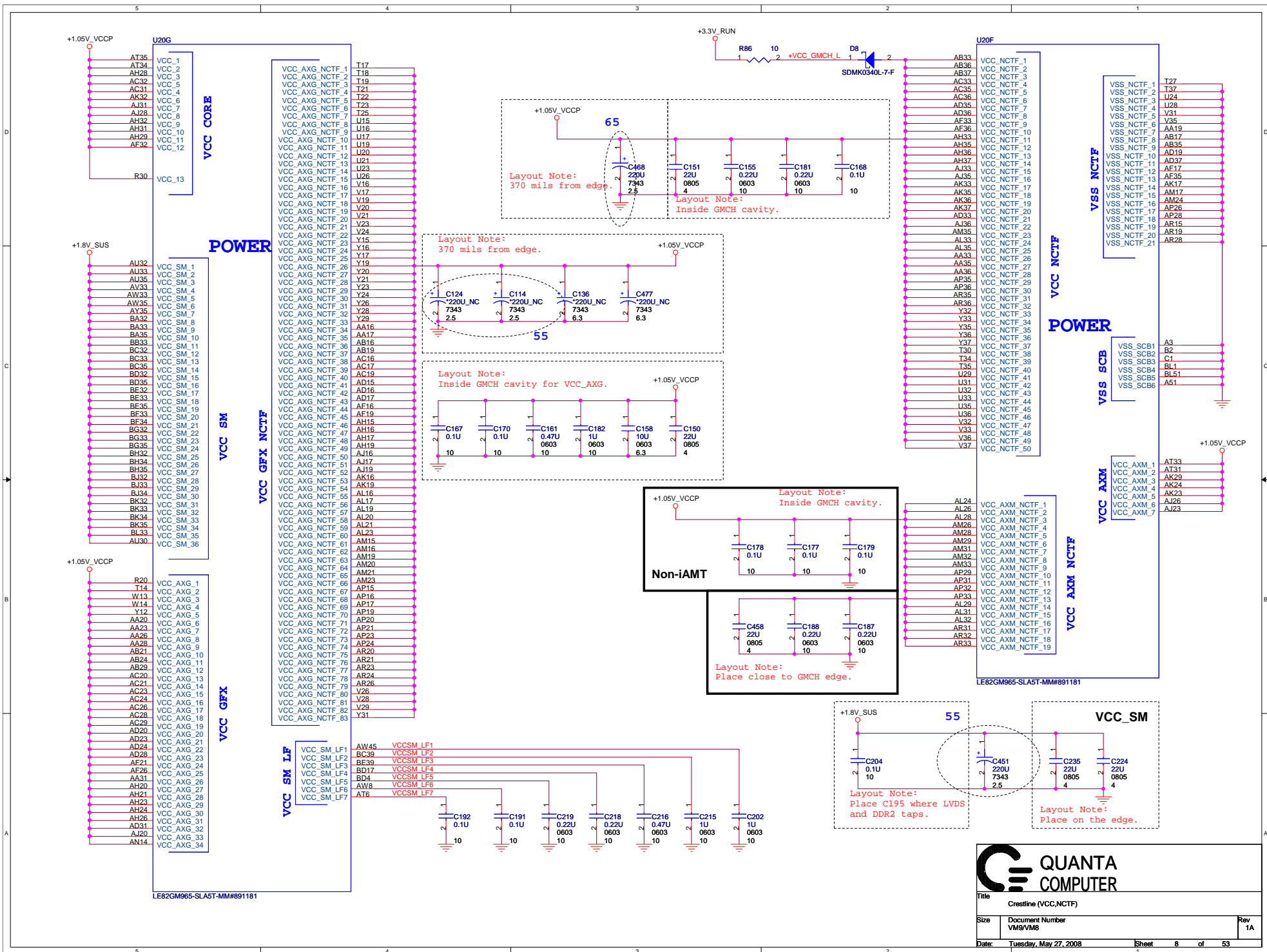
- ET42 1 DDR A CAS#
  - ET37 1 DDR A RAS#
  - ET31 1 DDR A WE#
  - ET39 1 DDR CS0 DIMMA#
  - ET32 1 DDR A MA#
  - ET28 1 DDR A DQS0
  - ET27 1 DDR A DQS#0
  - ET23 1 DDR A D5
  - ET28 1 DDR A D22
  - ET40 1 DDR A D22
- DDR\_CS0\_DIMMA# 6,15,16

76: For EA test use

- ET36 1 DDR B CAS#
  - ET37 1 DDR B RAS#
  - ET33 1 DDR B WE#
  - ET38 1 DDR CS3 DIMMB#
  - ET35 1 DDR B MA#
  - ET41 1 DDR B MA1
  - ET24 1 DDR B DQS0
  - ET25 1 DDR B DQS#0
  - ET30 1 DDR B D5
  - ET34 1 DDR B D41
  - ET43 1 DDR B D41
- DDR\_CS3\_DIMMB# 6,15,16



Title			Crestline (DDR2)
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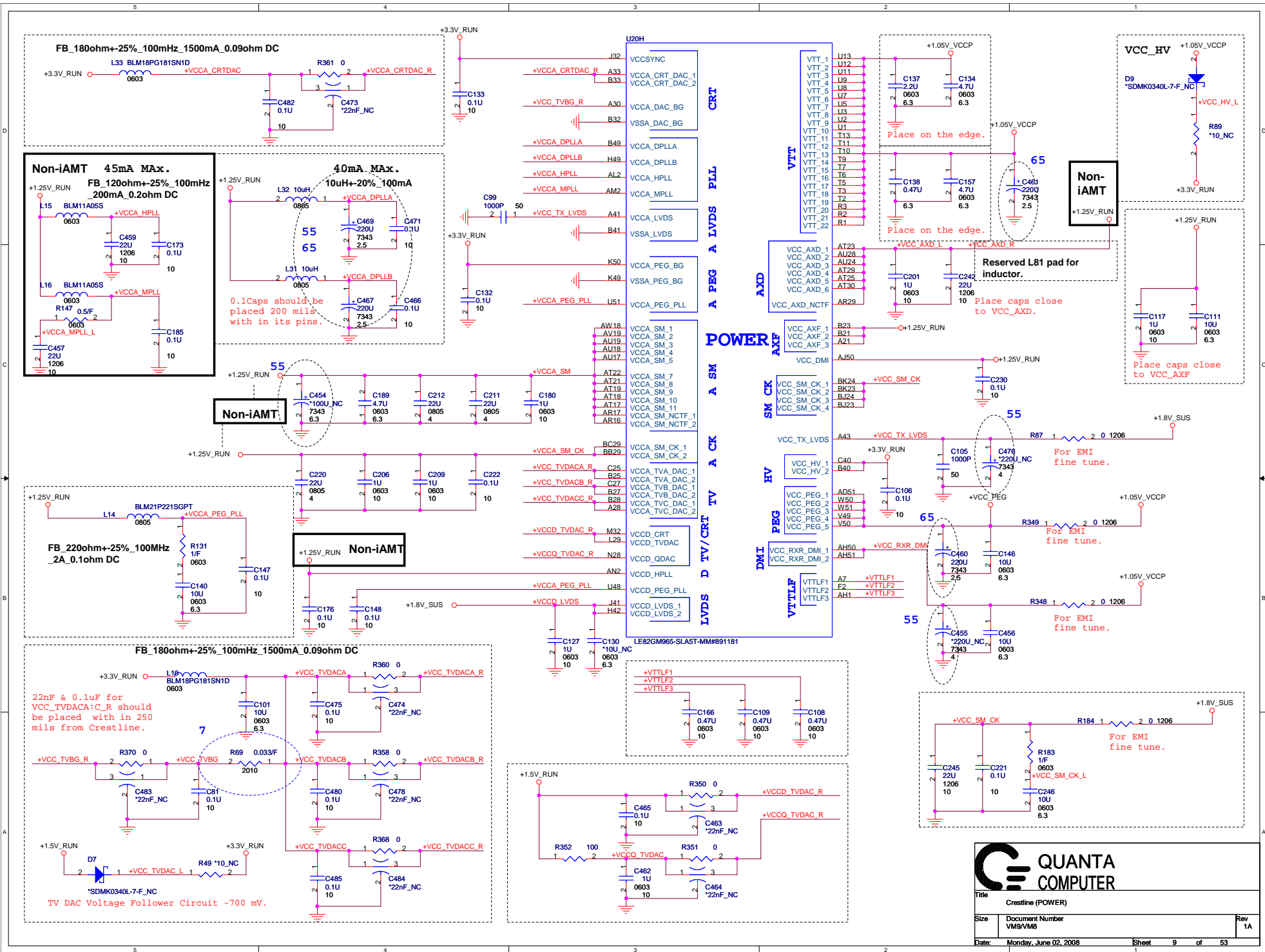
LE82GM965-SLA5T-MM#891181

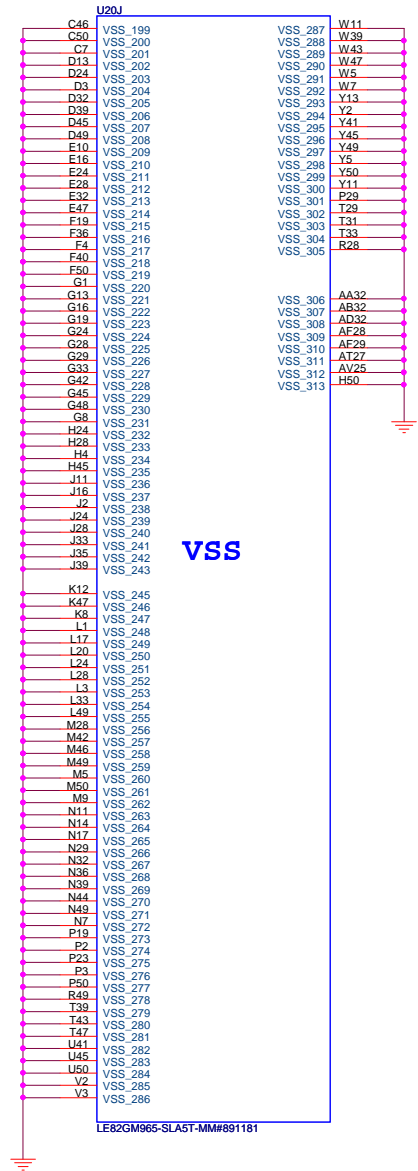
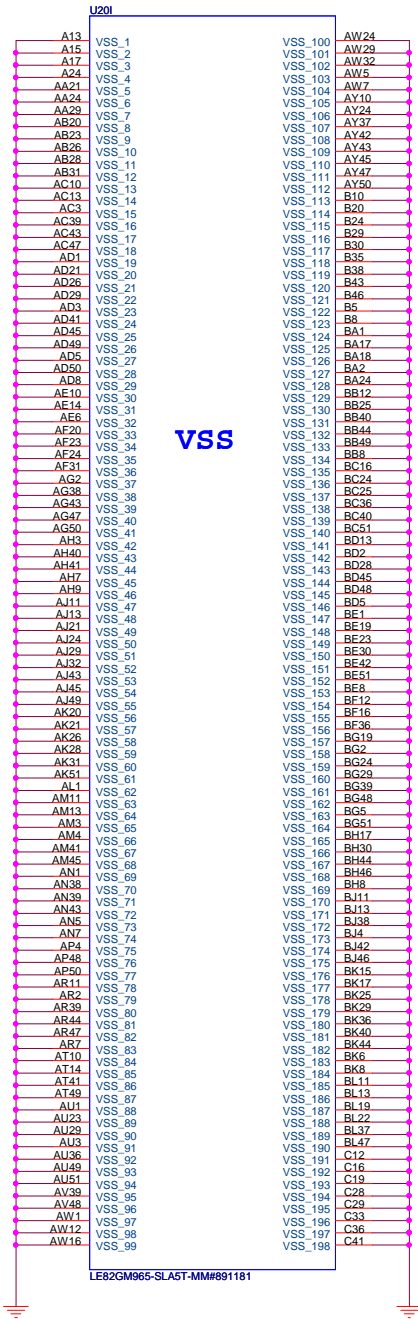
**QUANTA COMPUTER**

Title: Crestline (VCC,NCTF)

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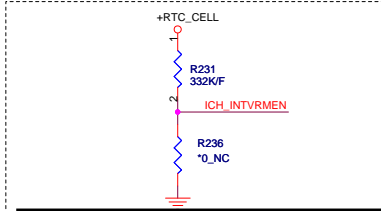
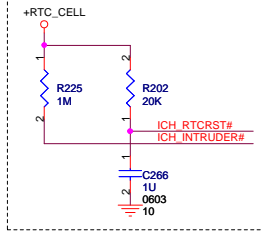
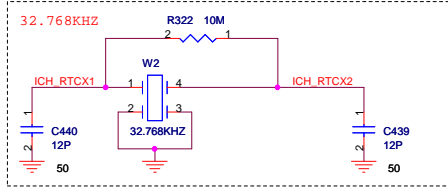


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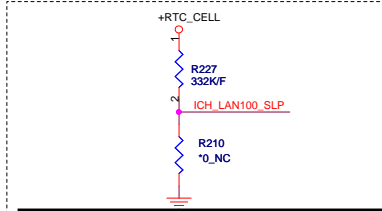
Title: Crestline (VSS)

Size	Document Number VM9/VM8	Rev 1A
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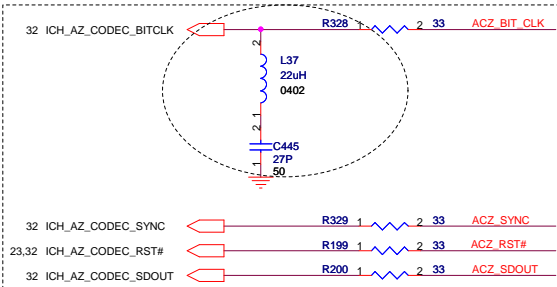
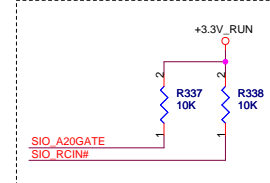
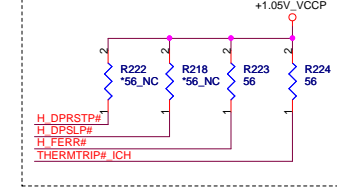
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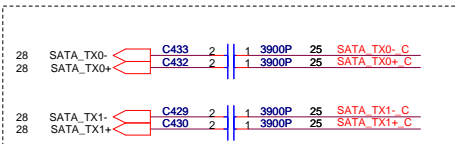
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)



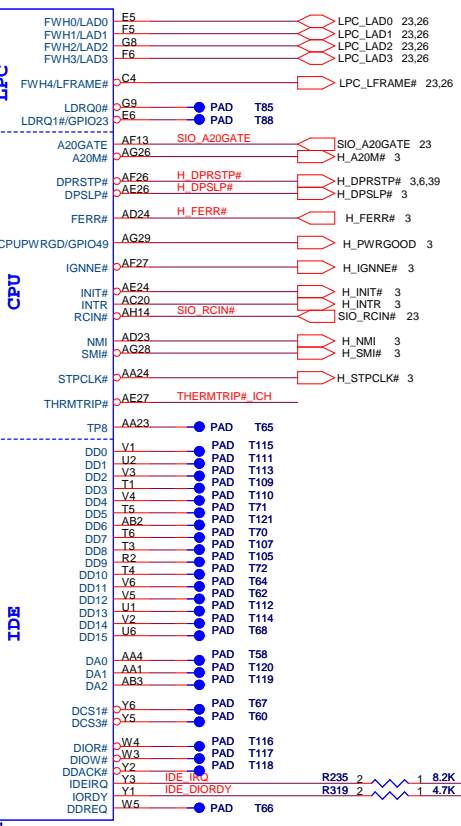
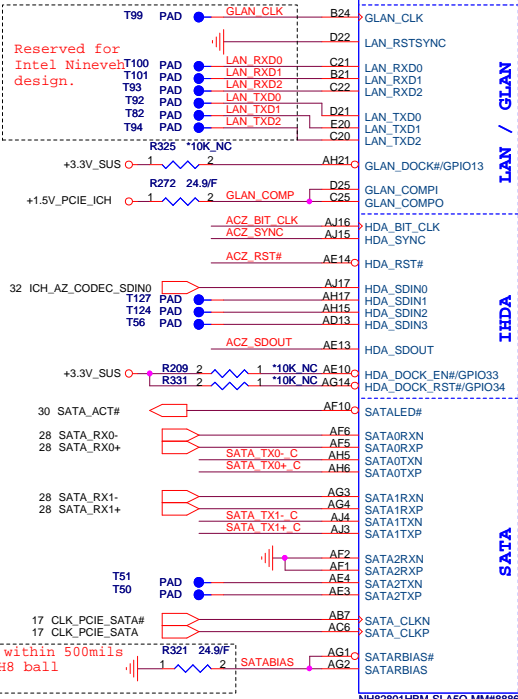
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source.

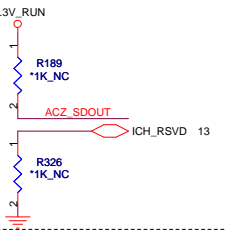


Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.



Place within 500mils of ICH8 ball

XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOU	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



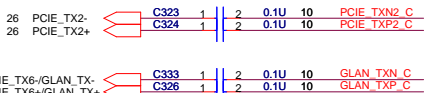
**QUANTA COMPUTER**

Title: ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)

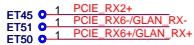
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Place TX DC blocking caps close ICH8.

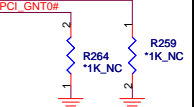


For EA test use



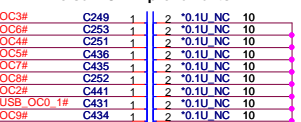
76

ICH\_SPL\_CS1#\_R

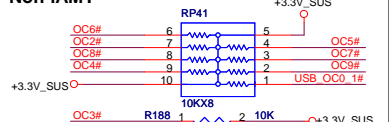


	GNT0#	SPI_CS1#
LPC	11	No stuff
PCI	10	No stuff
SPI	01	Stuff

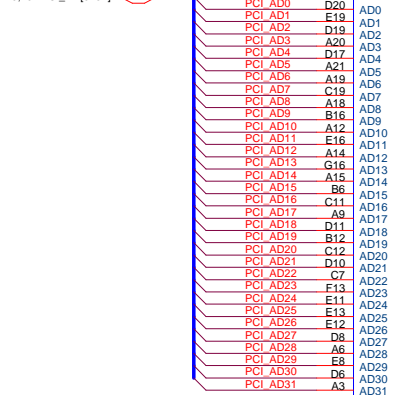
WWAN Noise - ICH improvements



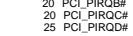
Non-iAMT



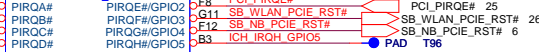
20.25 PCI\_AD[0..31]



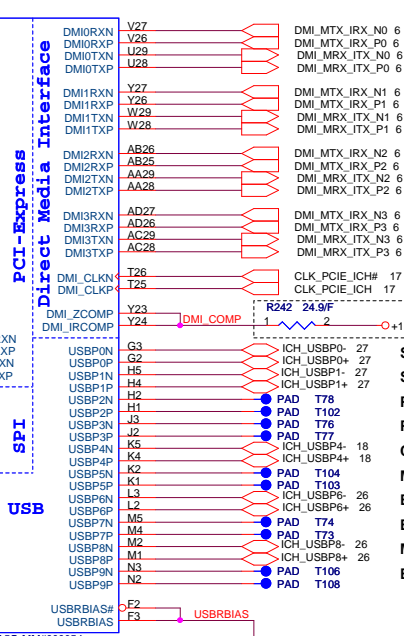
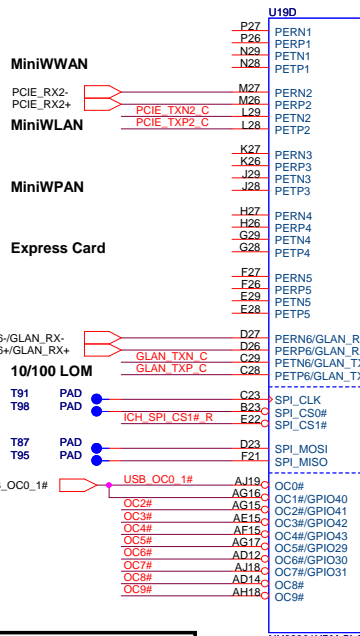
20 PCI\_PIRQA#



Interrupt I/F



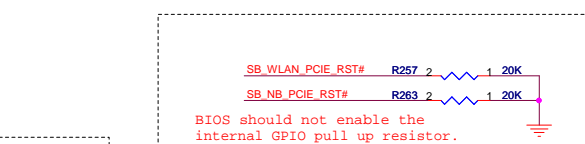
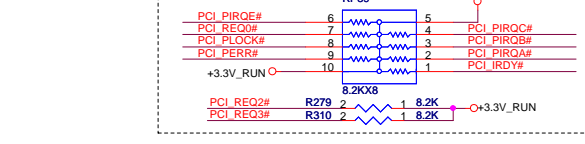
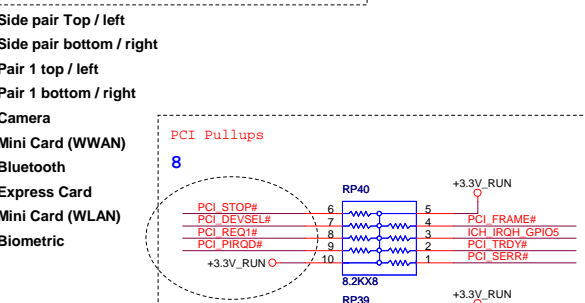
NH82801HBM-SLA50-MM#888654



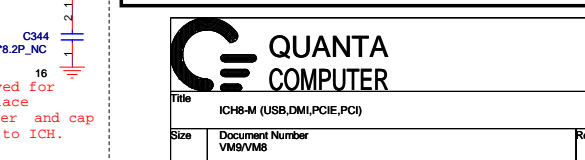
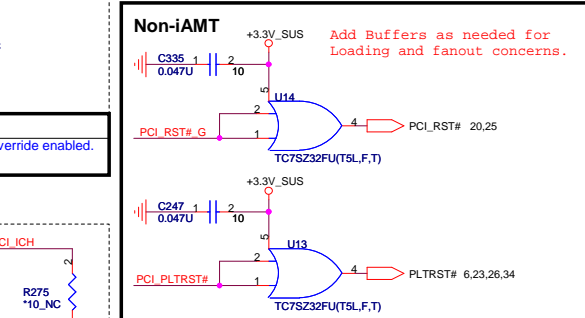
Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.



Place within 500mils of ICH8



BIOS should not enable the internal GPIO pull up resistor.



Reserved for EMI. Place resistor and cap close to ICH.

**QUANTA COMPUTER**

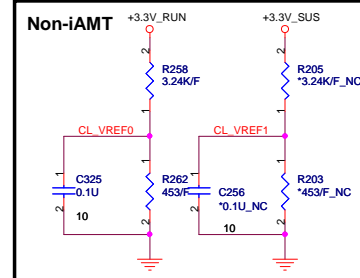
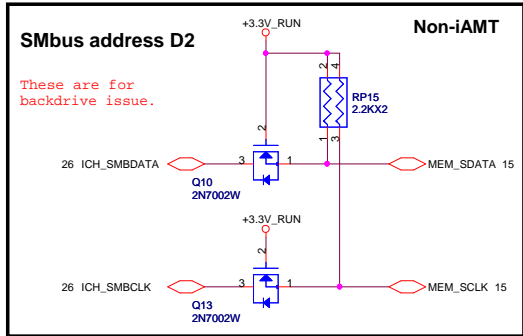
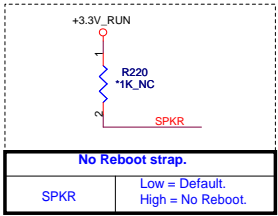
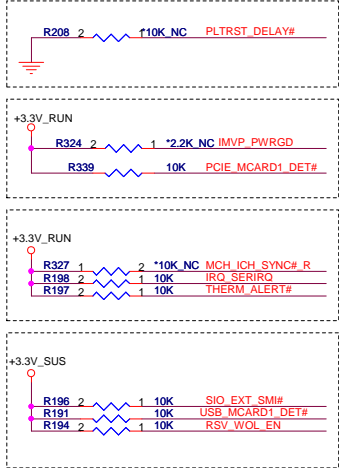
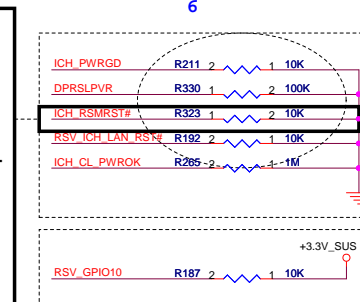
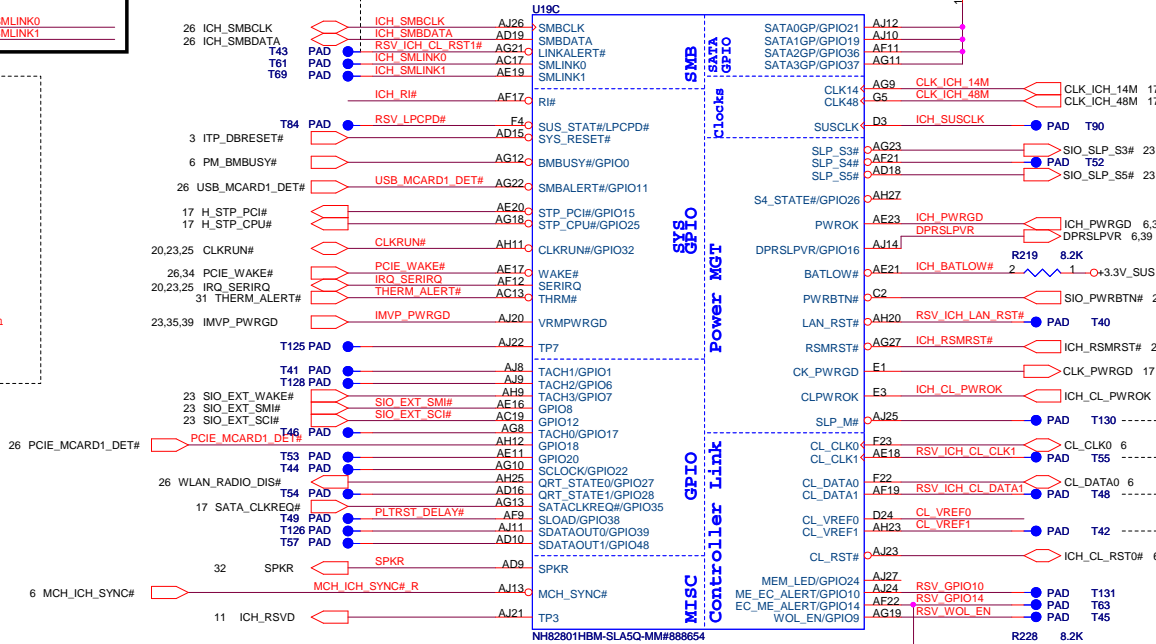
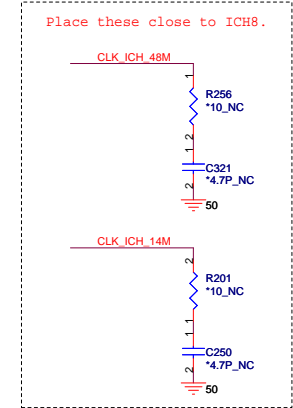
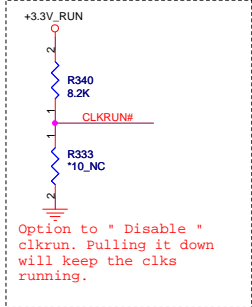
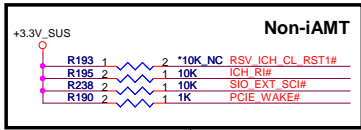
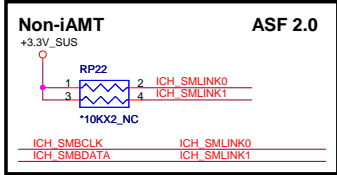
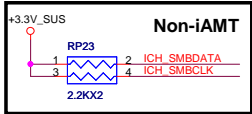
Title: ICH8-M (USB,DMI,PCIE,PCI)

Size: Document Number VMS/VMB

Rev: 1A

Date: Friday, May 30, 2008

Sheet: 12 of 53



**QUANTA COMPUTER**

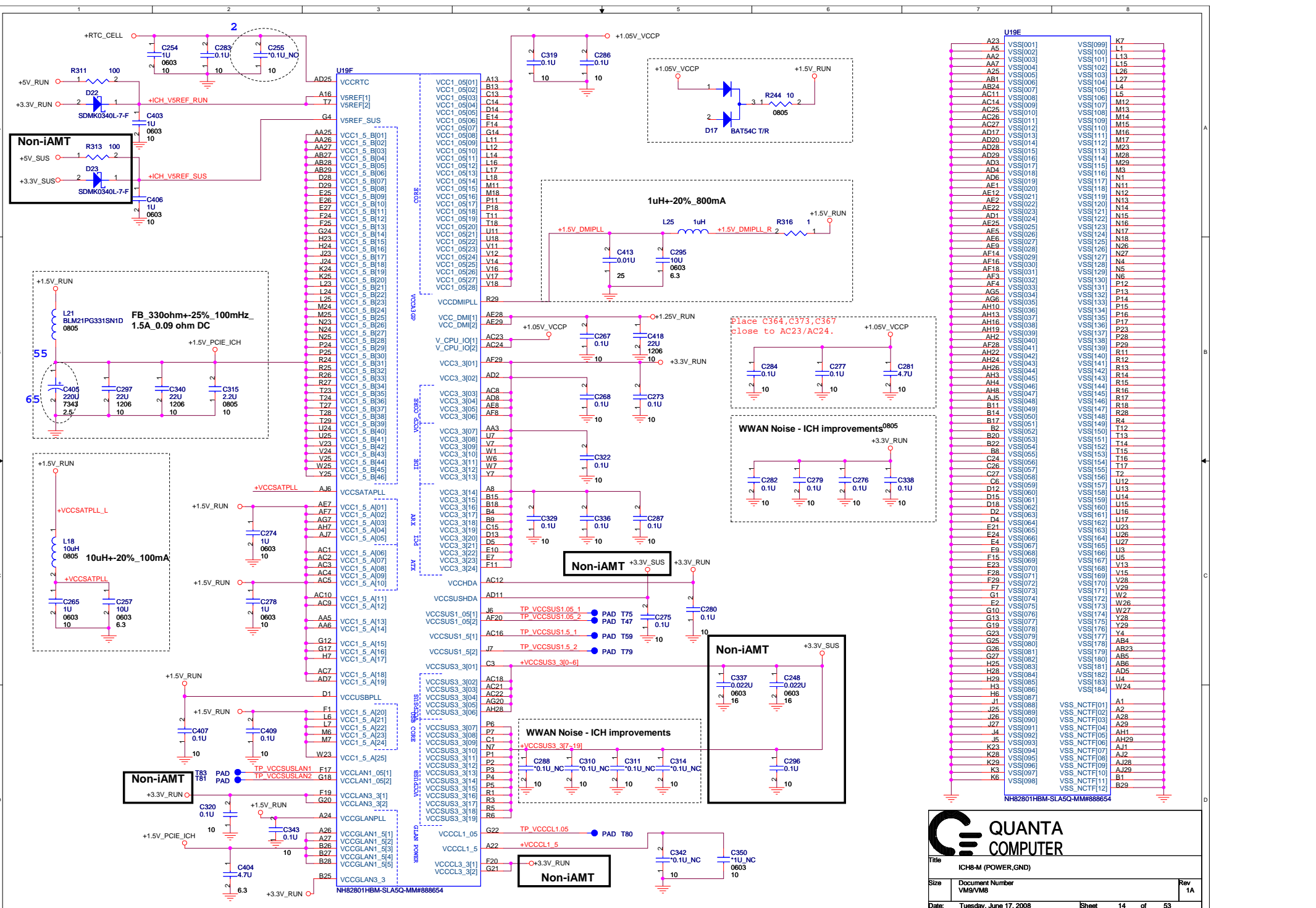
Title: ICH8-M (PM,GPIO,SMB,CL)

Size: Document Number VM9/VMB

Date: Saturday, June 21, 2008

Sheet: 13 of 53

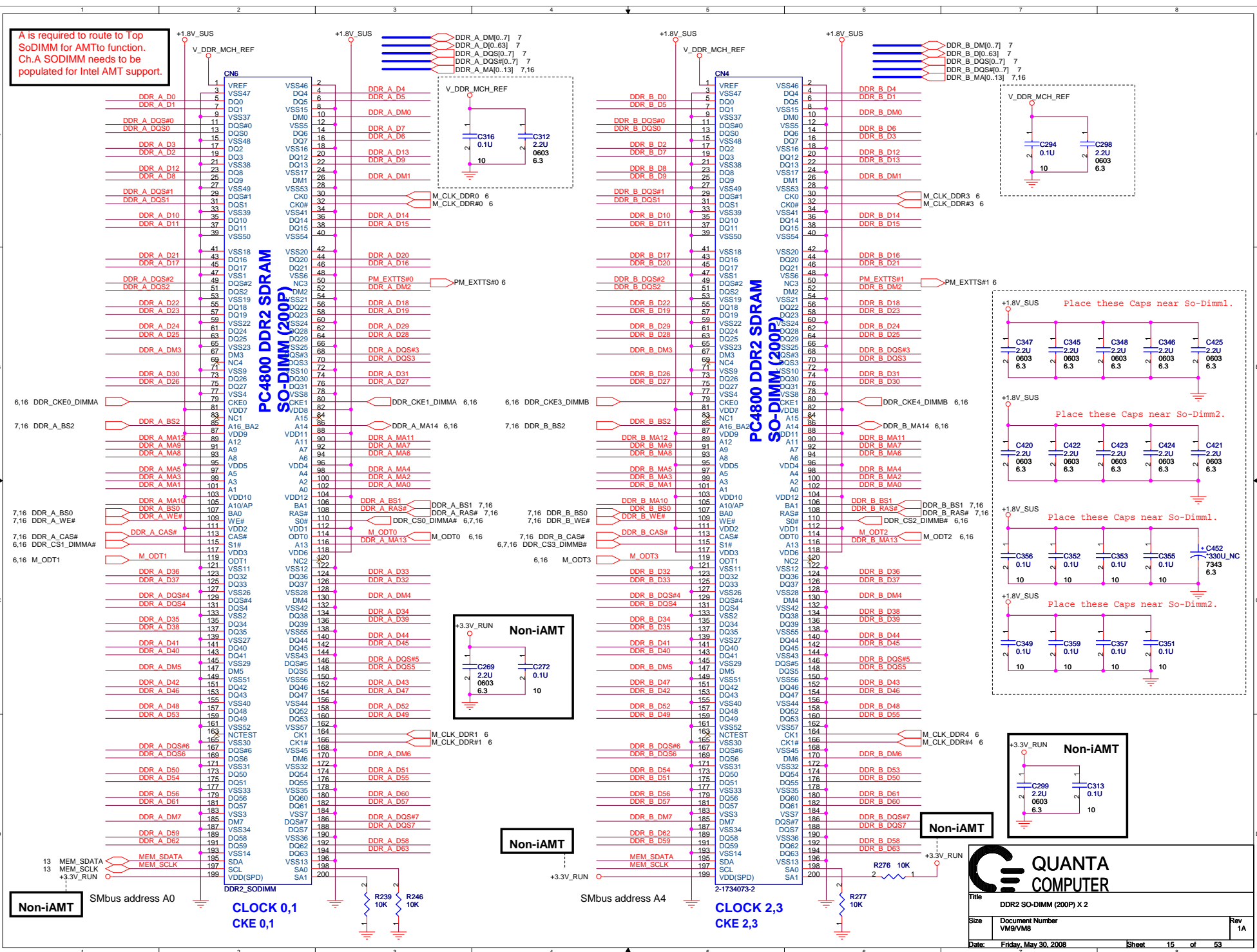
Rev: 1A



**QUANTA COMPUTER**

Title: ICH8-M (POWER,GND)  
 Size: Document Number VMS/VMB Rev: 1A  
 Date: Tuesday, June 17, 2008 Sheet: 14 of 53

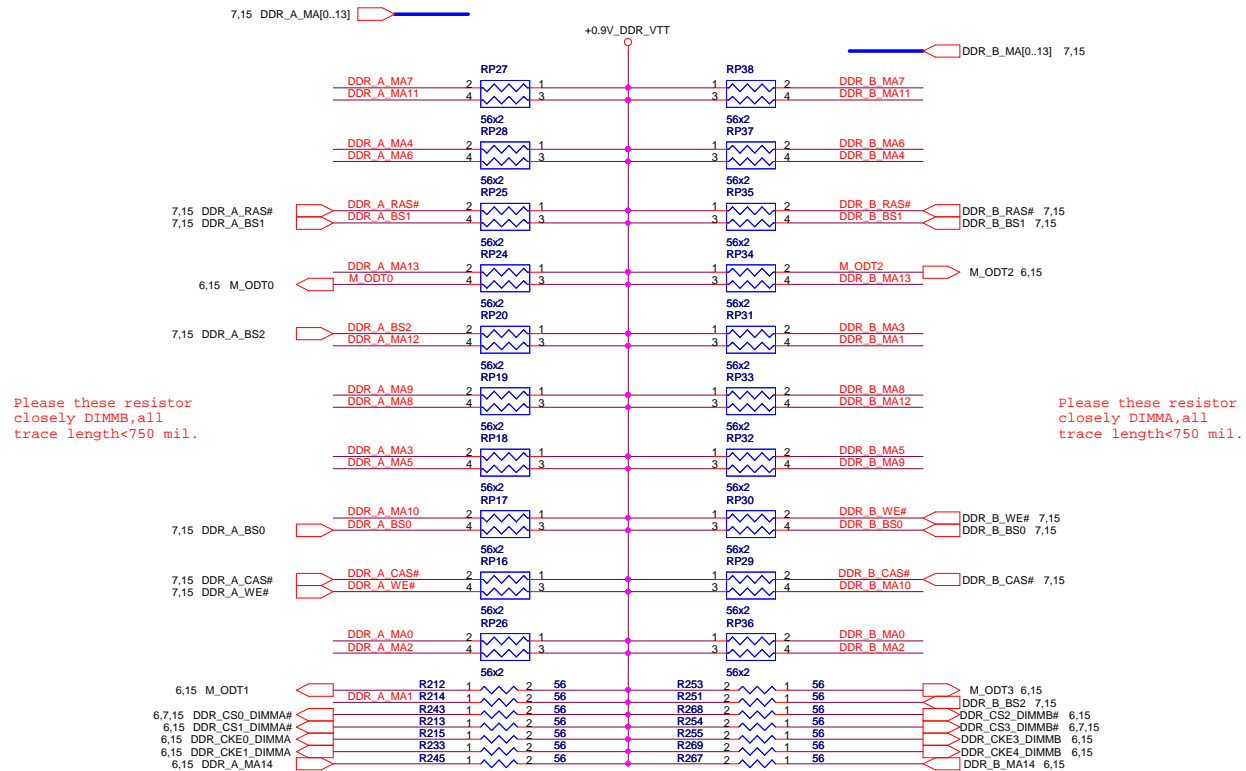
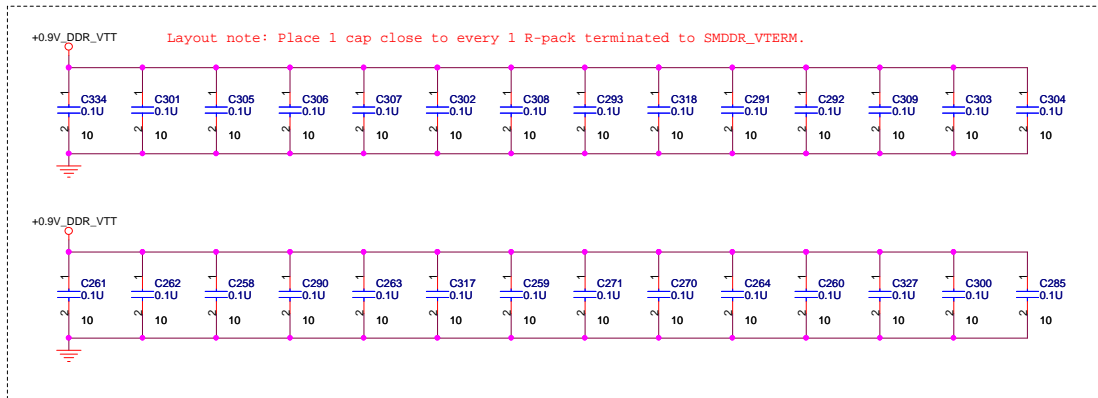
A is required to route to Top SoDIMM for AMT to function. Ch.A SODIMM needs to be populated for Intel AMT support.



**QUANTA COMPUTER**

Title: DDR2 SO-DIMM (200P) X 2

Size	Document Number V19/V18	Rev	1A
Date:	Friday, May 30, 2008	Sheet	15 of 53



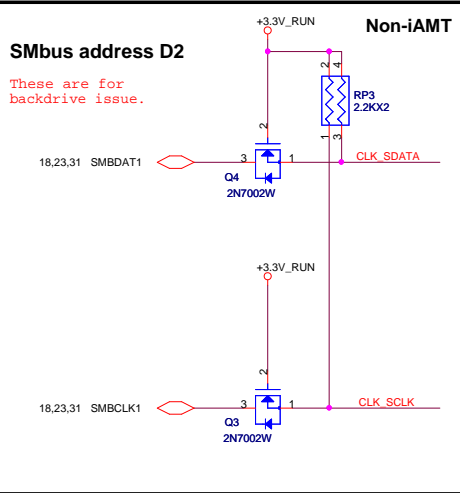
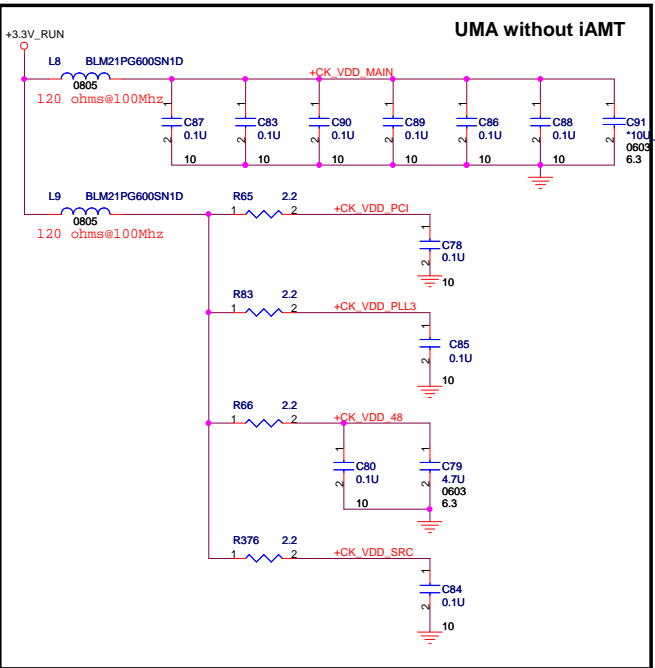
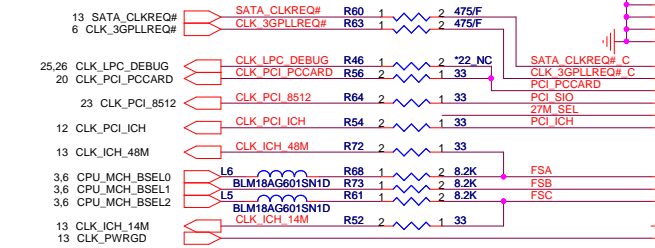
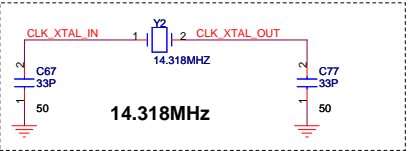
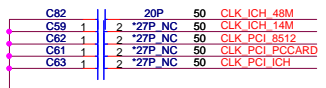
**QUANTA COMPUTER**

Title: DDR2 RES ARRAY

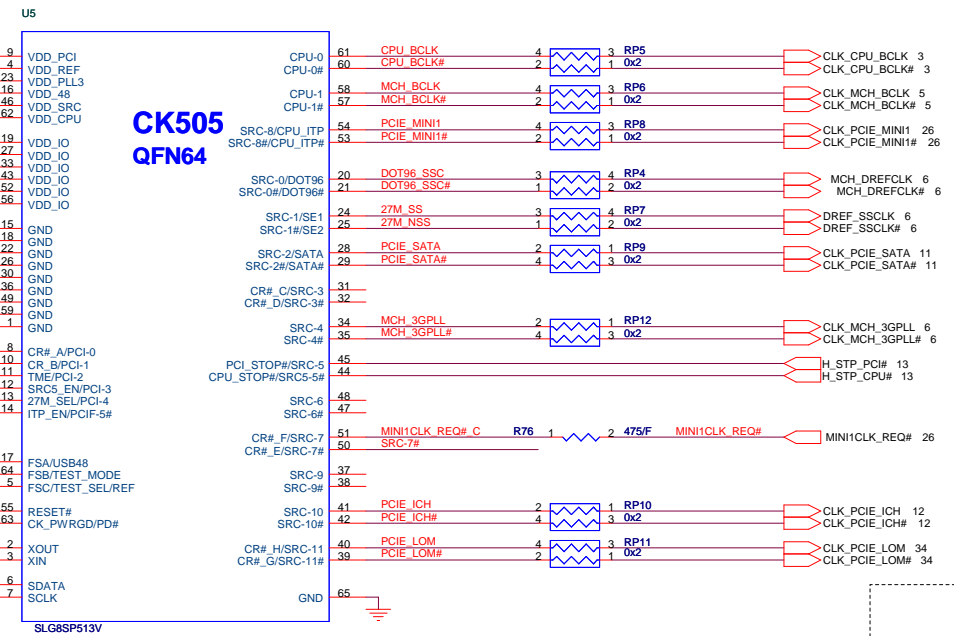
Size	Document Number VM9/VM8	Rev	1A
Date:	Friday, May 30, 2008	Sheet	16 of 53



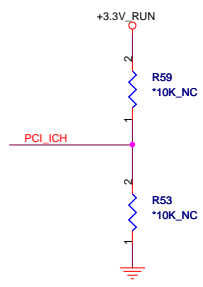
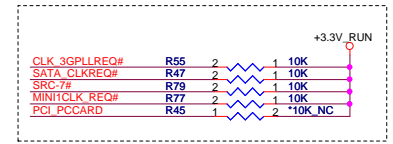
**Add capacitor pads for improving WWAN.**



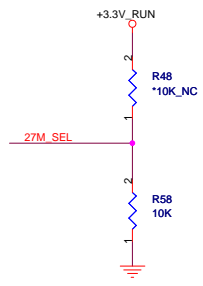
**CK505 QFN64**



Silego need pull up but other?



R185 POP: For Internal pull-low.  
R439 POP: For internal pull-high.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

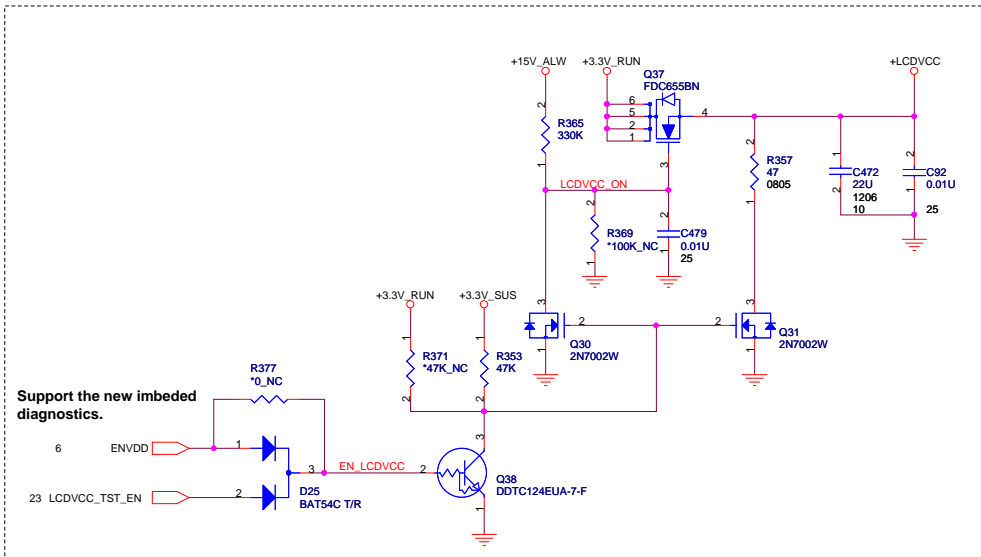
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GFRX down	SRCT0	SRCC0	27Mout	27MSSout

**QUANTA COMPUTER**

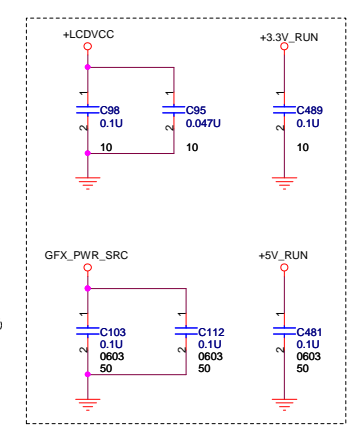
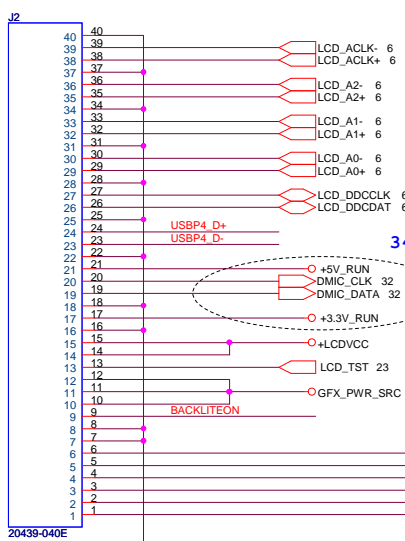
Title: CLOCK GENERATOR

Size: Document Number VM9/VM8 Rev 1A

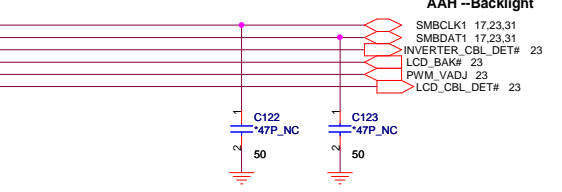
Date: Friday, May 30, 2008 Sheet 17 of 53



Support the new imbedded diagnostics.



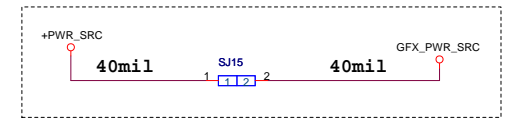
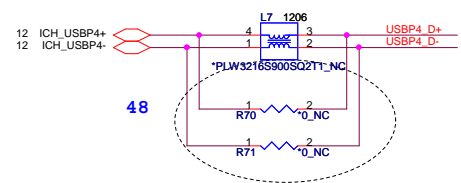
Adres : A9H -- Contrast  
AAH -- Backlight

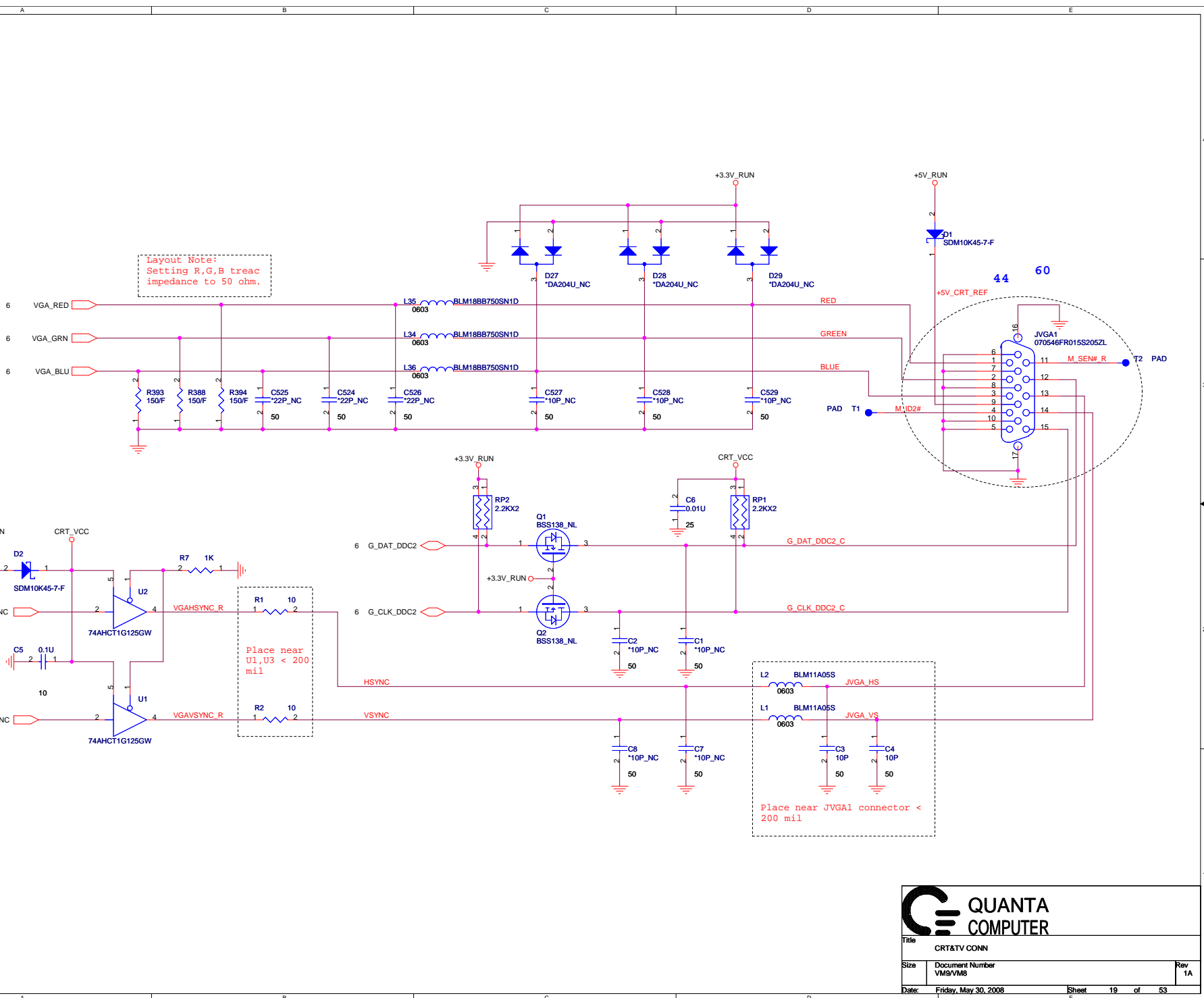


**UMA**

Populate R351 for DPST implementation only.

Populate R346 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.





Layout Note:  
Setting R,G,B trace  
impedance to 50 ohm.

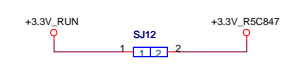
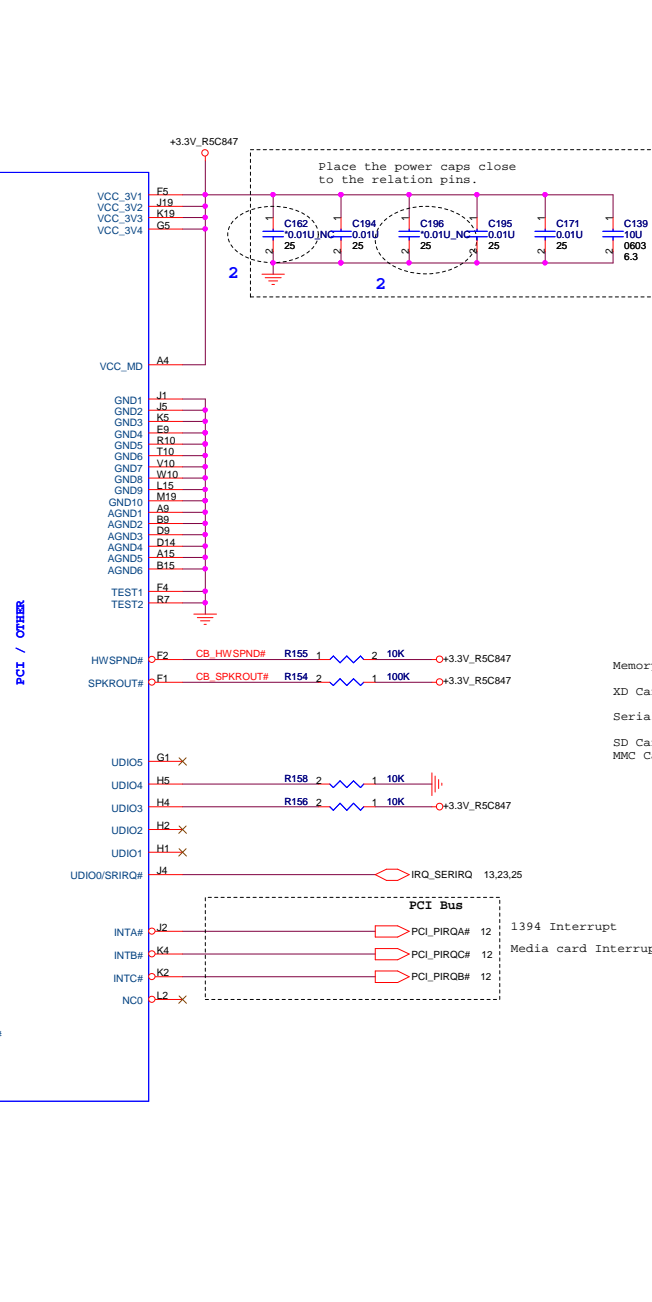
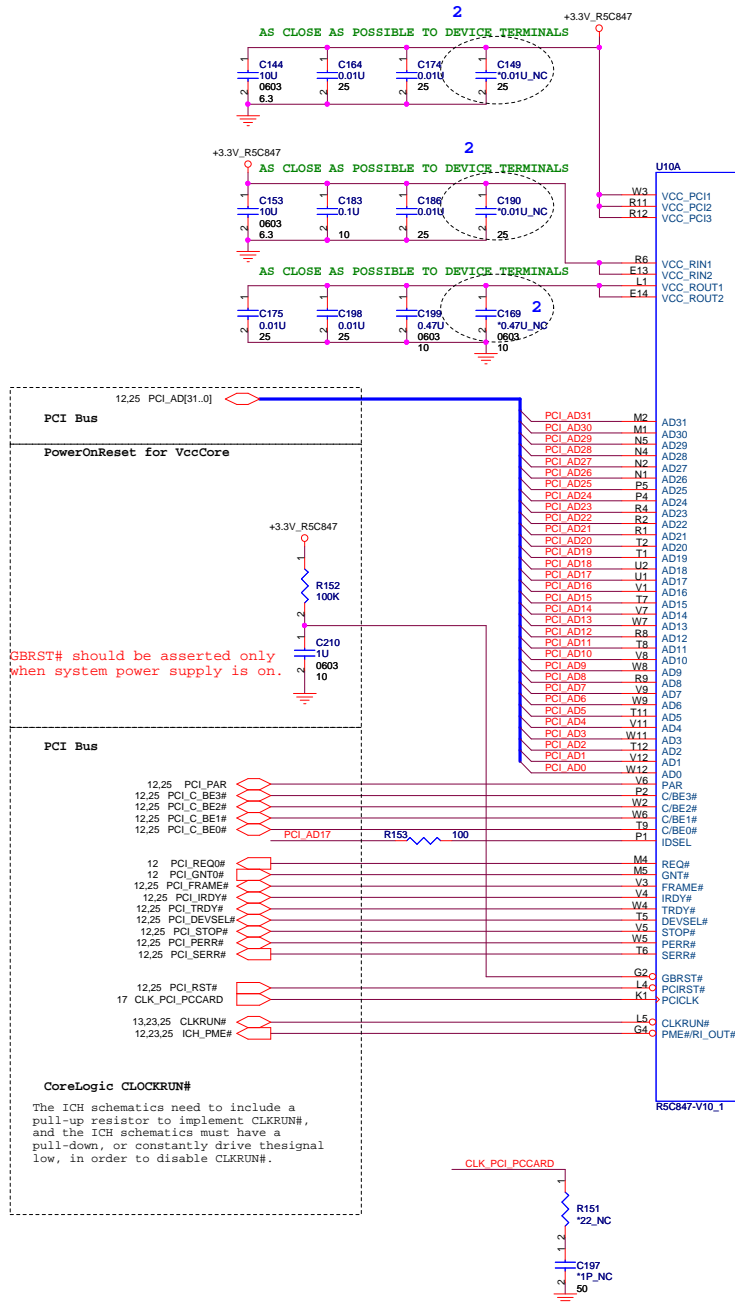
Place near  
U1,U3 < 200  
mil

Place near JVGA1 connector <  
200 mil

**QUANTA COMPUTER**

Title: CRT&TV CONN

Size	Document Number VM9/VM8	Rev 1A
Date:	Friday, May 30, 2008	Sheet 19 of 53

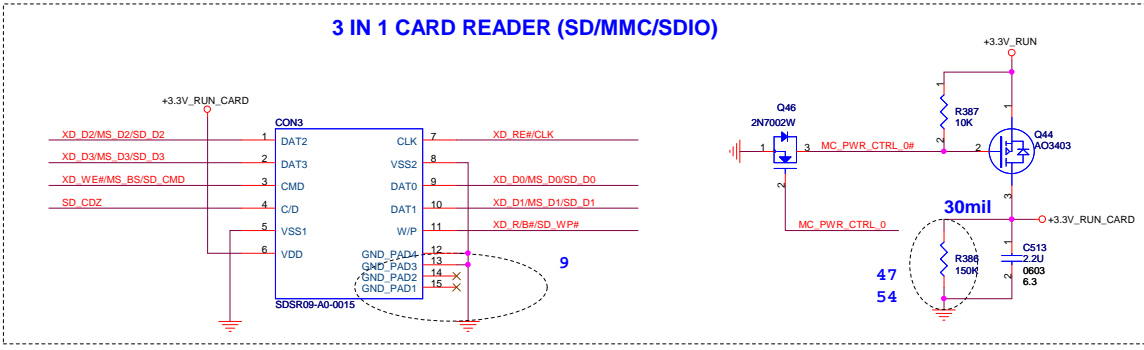
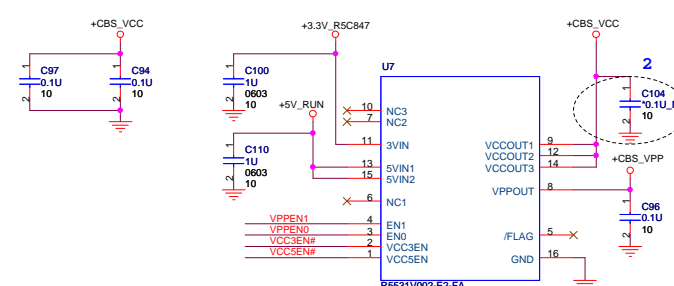
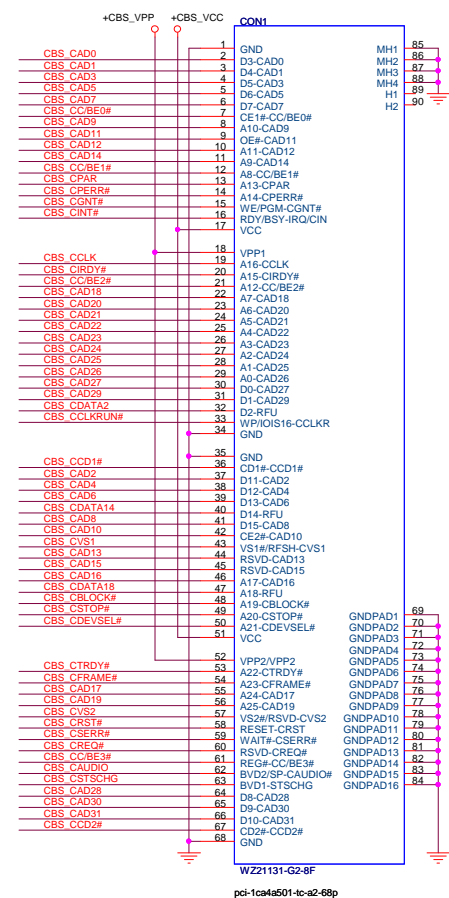
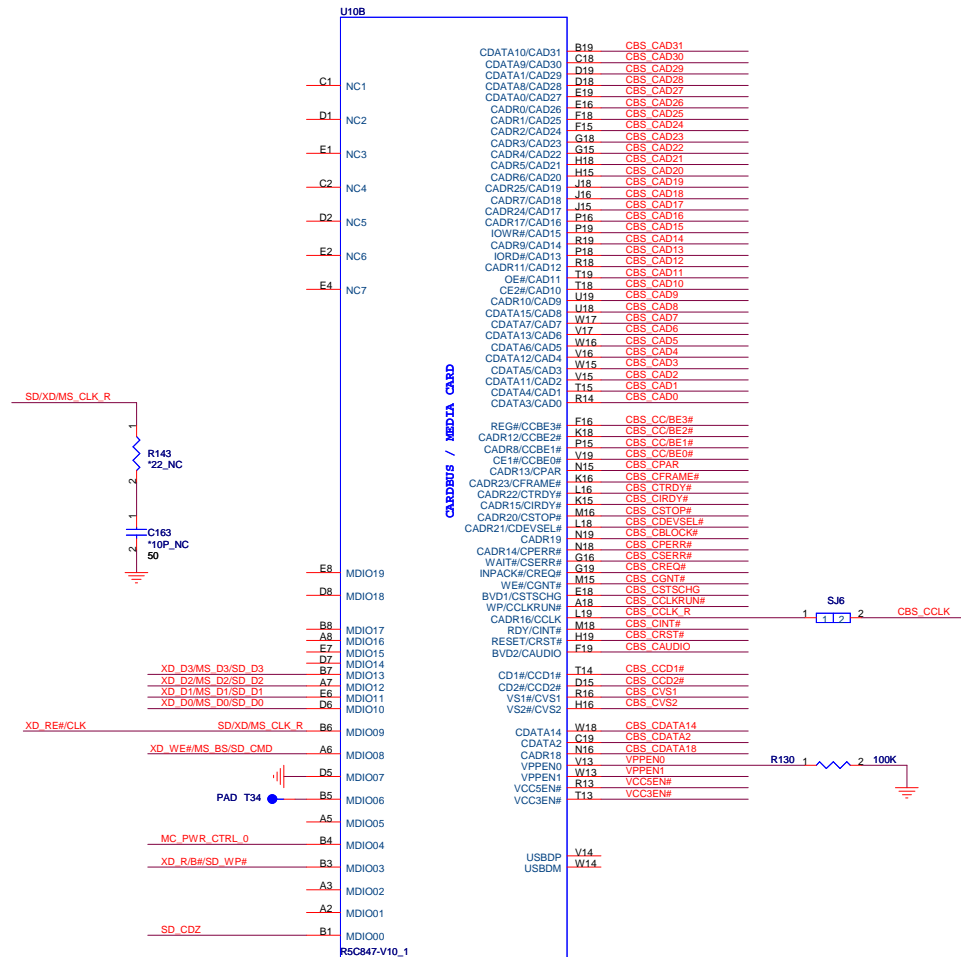


GBRST# should be asserted only when system power supply is on.

- Memory Stick Enable
- XD Card Enable
- Serial ROM disable
- SD Card Enable
- MMC Card Enable

**CoreLogic CLOCKRUN#**  
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

QUANTA COMPUTER		
Title	S IN 1 CONTROLLER	
Size	Document Number VMS/VMB	Rev 1A
Date:	Tuesday, June 17, 2008	Sheet 20 of 53



**QUANTA COMPUTER**

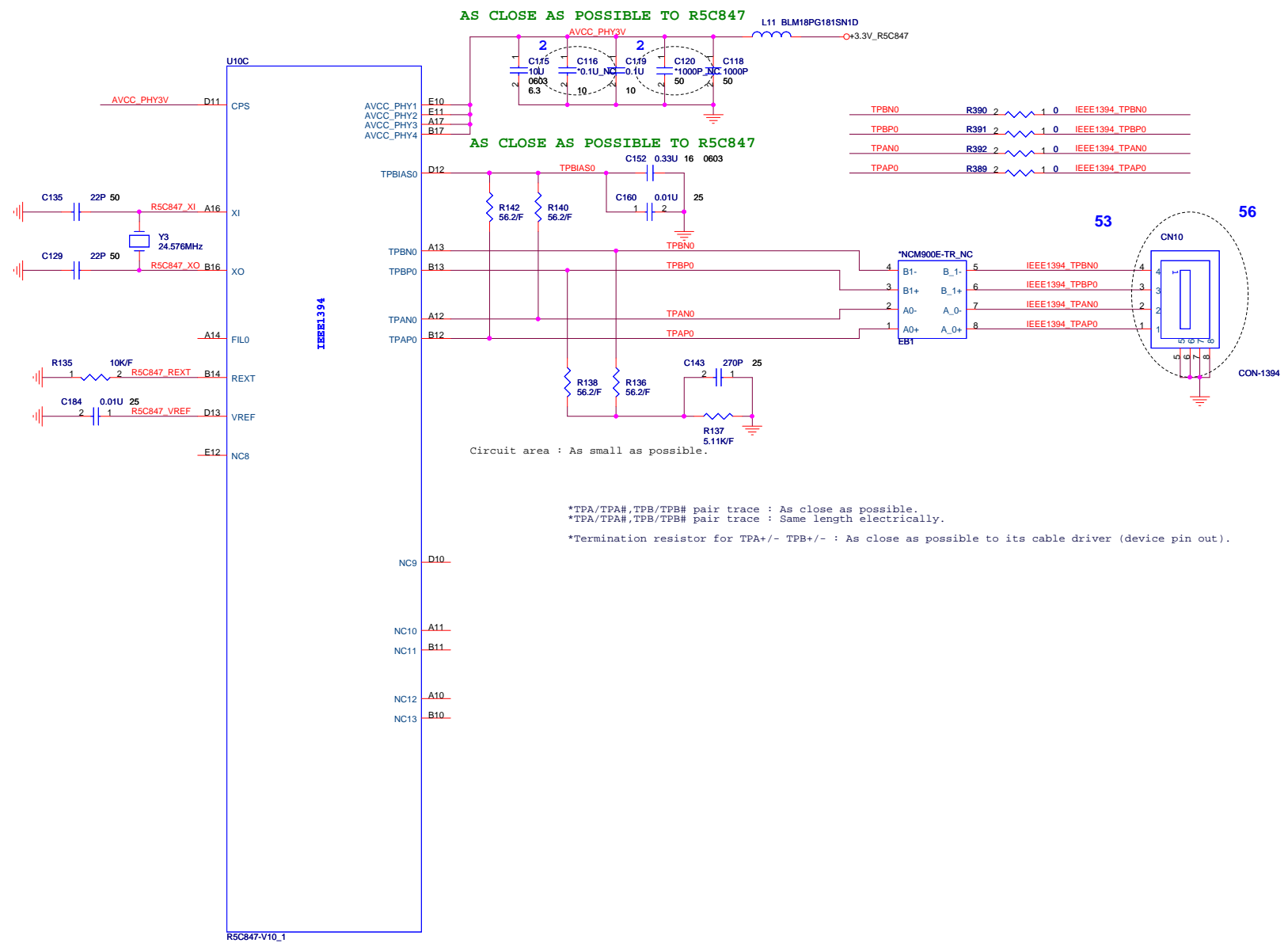
File: IEEE 1394

Size: Document Number VMS/VMB

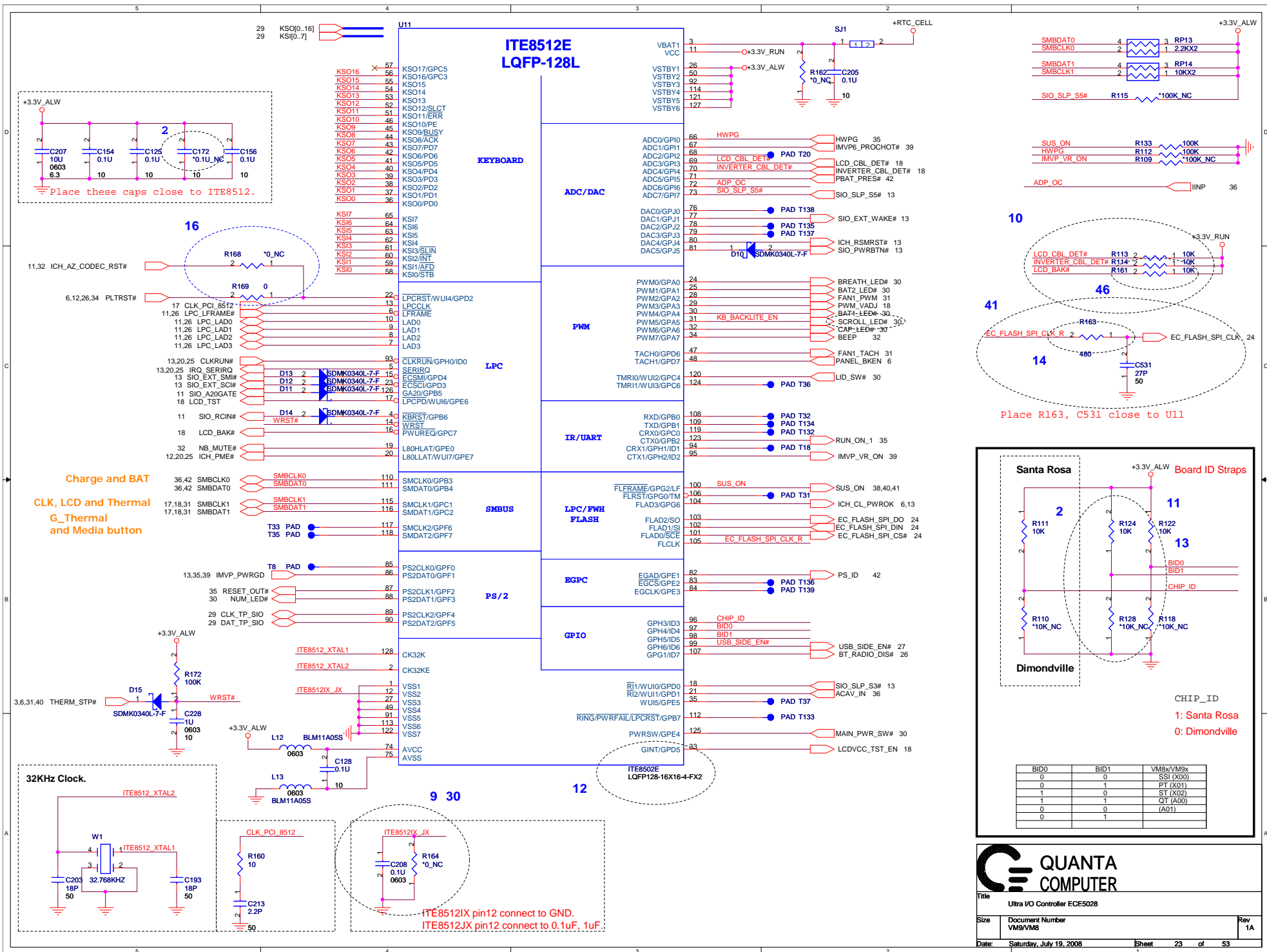
Date: Monday, June 23, 2008

Sheet: 21 of 53

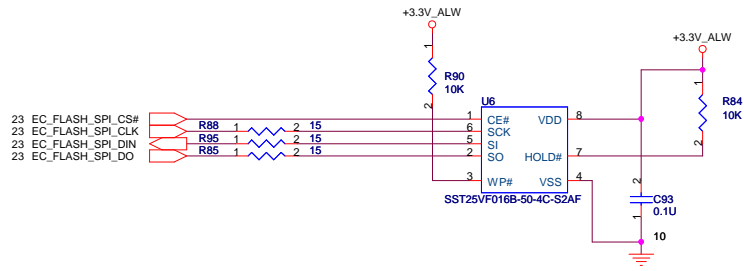
Rev: 1A



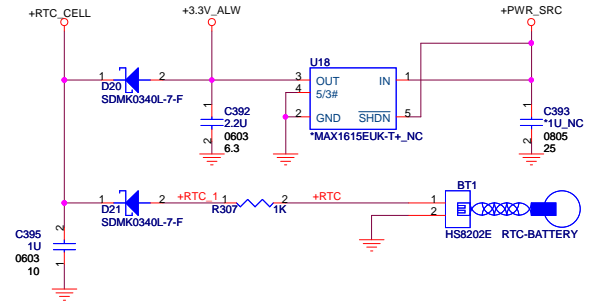
<b>QUANTA COMPUTER</b>		Title	
		ExpressCard/SmartCard	
Size	Document Number	Rev	
	VM9/VM8	1A	
Date: Tuesday, June 17, 2008		Sheet	22 of 53




16Mbit (2M Byte), SPI

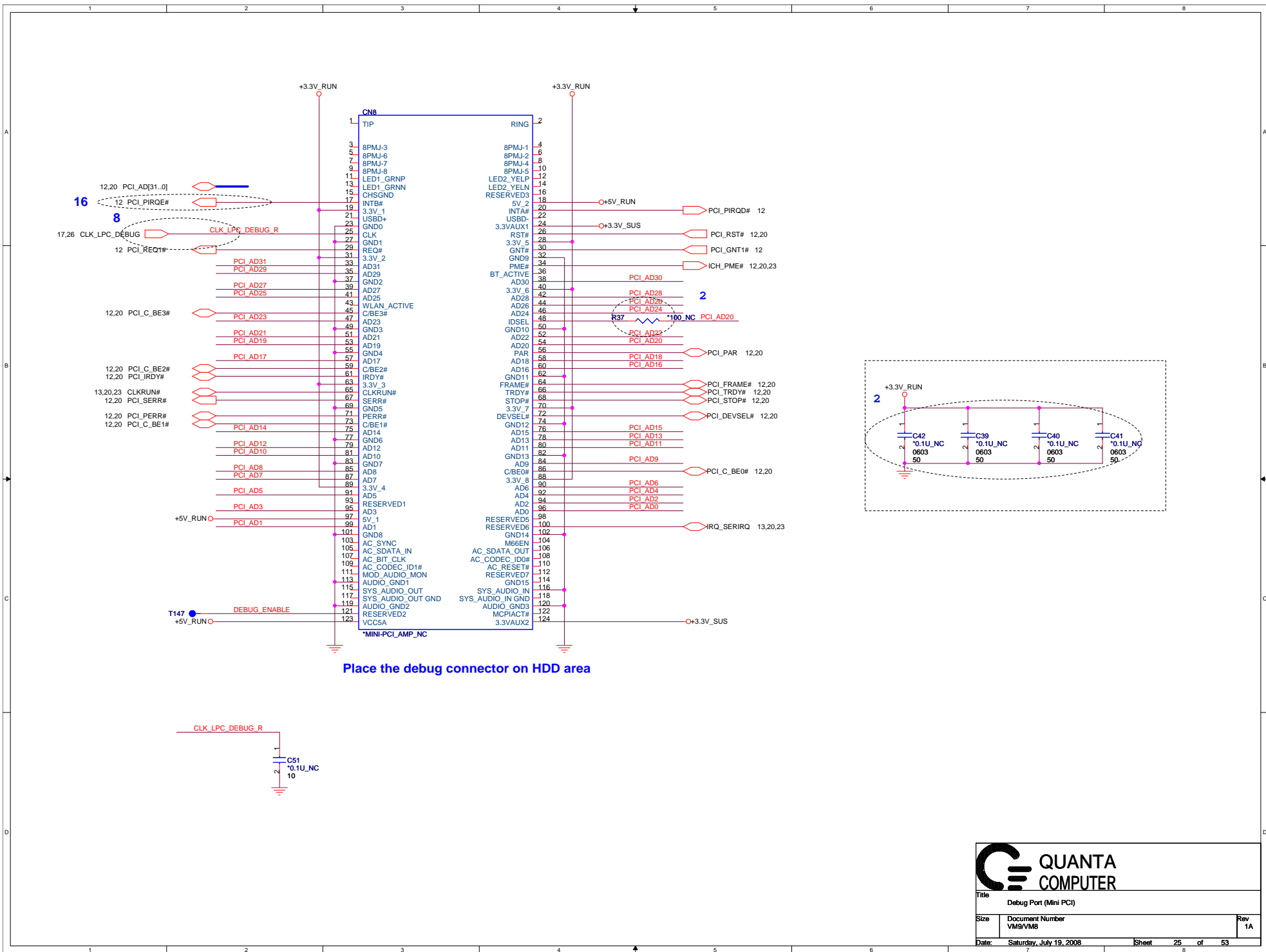


RTC BATTERY

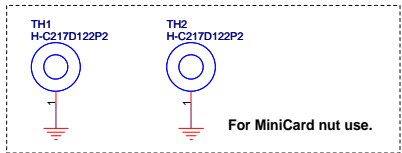


 <b>QUANTA COMPUTER</b>		Title	
		Ultra I/O Controller ECE5028	
Size	Document Number	Rev	
	VM9/VM8	1A	
Date:	Friday, May 30, 2008	Sheet	24 of 53

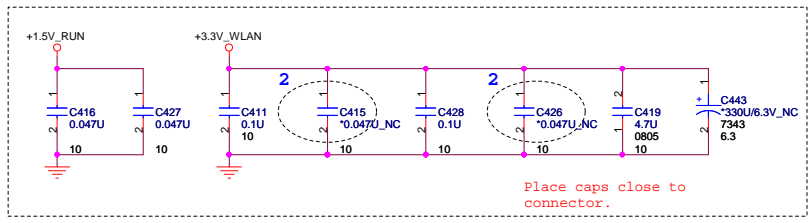
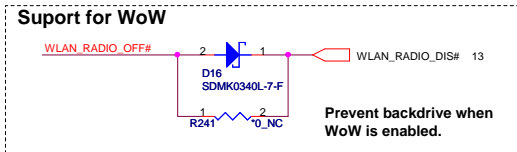
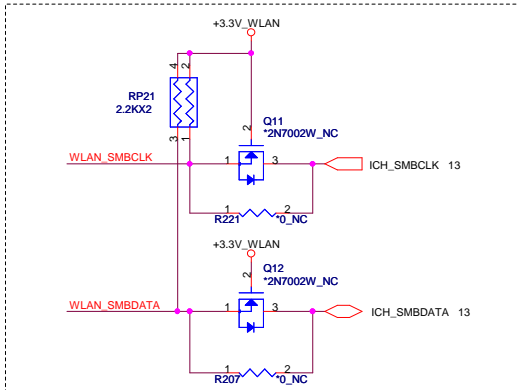
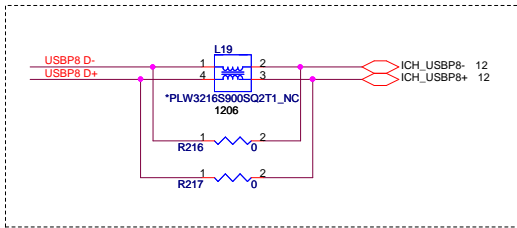
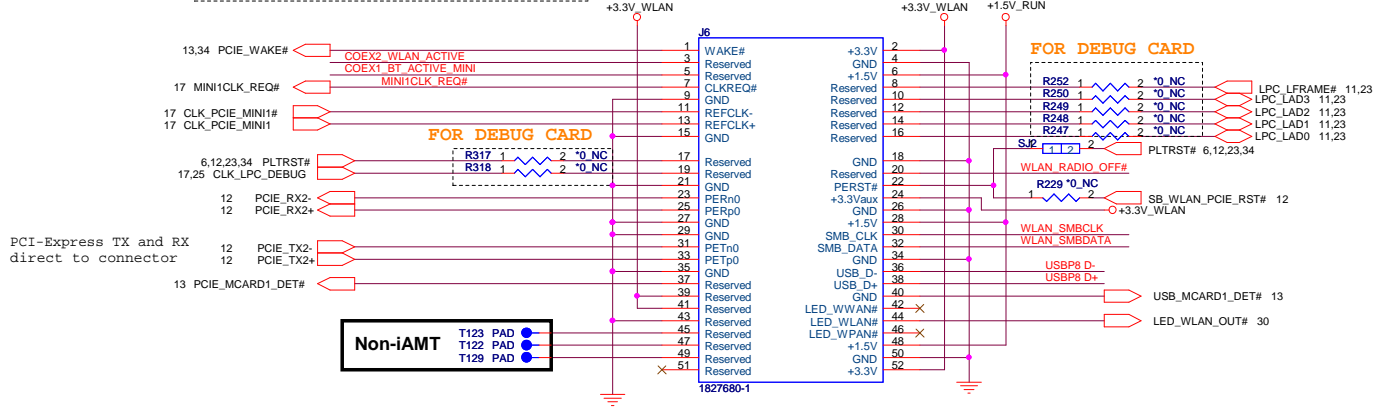




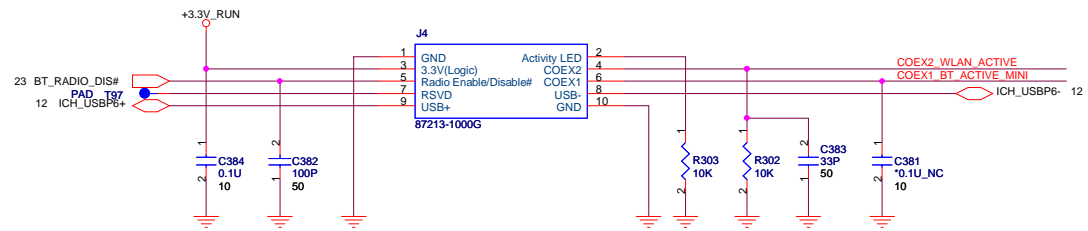
Title: Debug Port (Mini PCI)		
Size: VM9/VM8	Document Number: VM9/VM8	Rev: 1A
Date: Saturday, July 19, 2008	Sheet: 25	of 53



### MiniCard WLAN connector



### Bluetooth



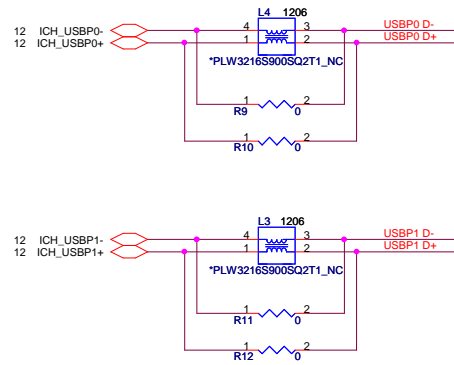
**QUANTA COMPUTER**

Title: MDC CONN.

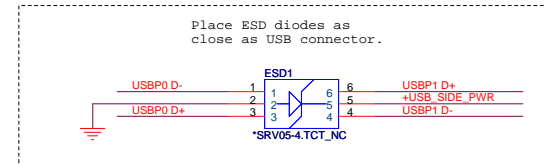
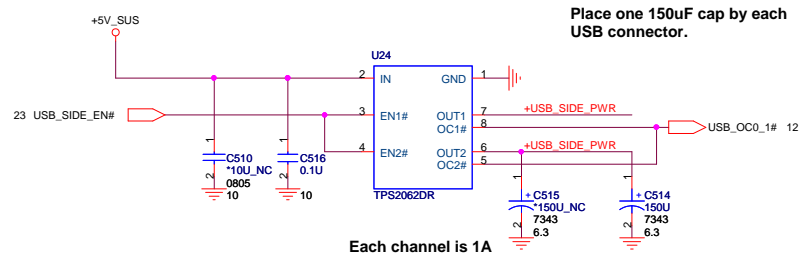
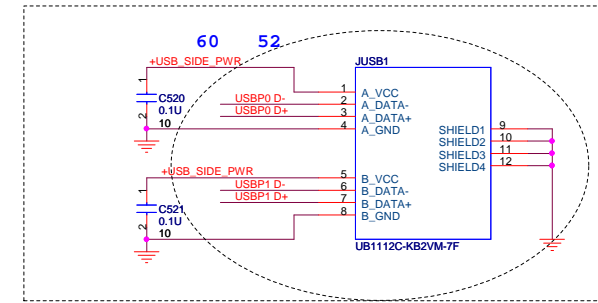
Size	Document Number VM9/VM8	Rev	1A
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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

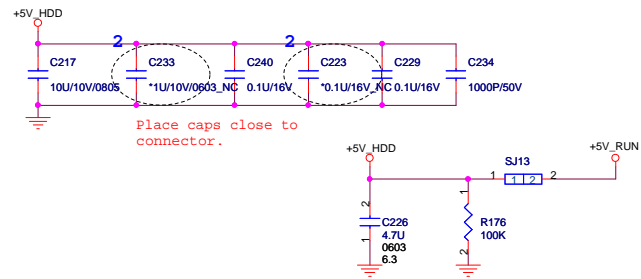
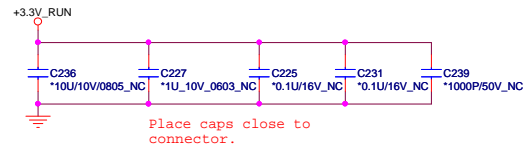
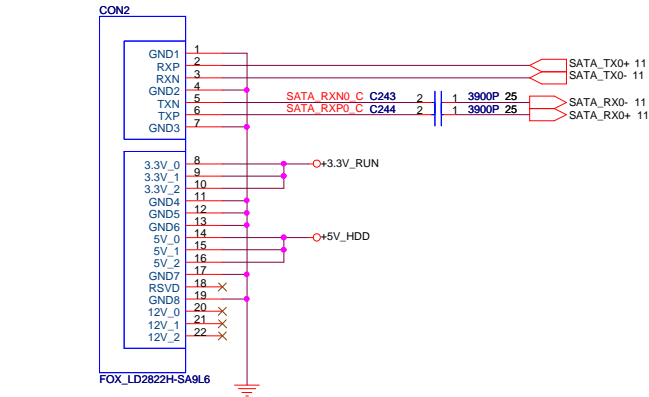


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

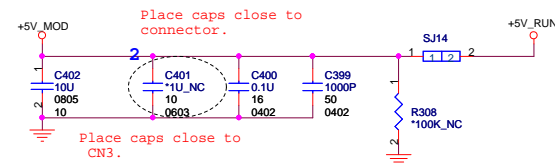
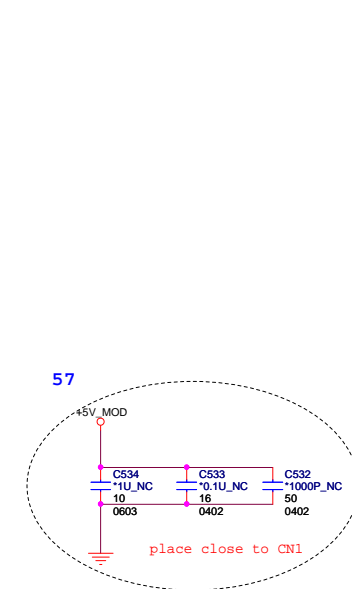
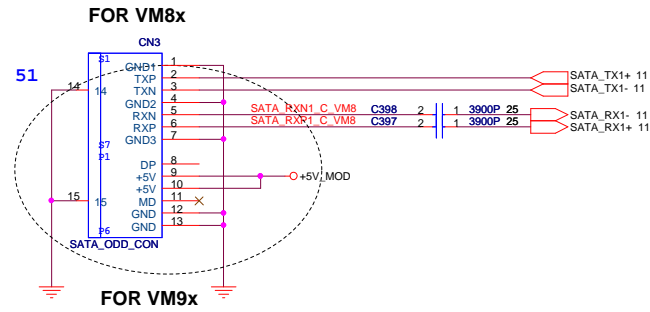


Title			SERIAL PORT & USB
Size	Document Number	Rev	
	VM9/VM8	1A	
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**SATA HDD Connector.**



**SATA ODD Connector.**

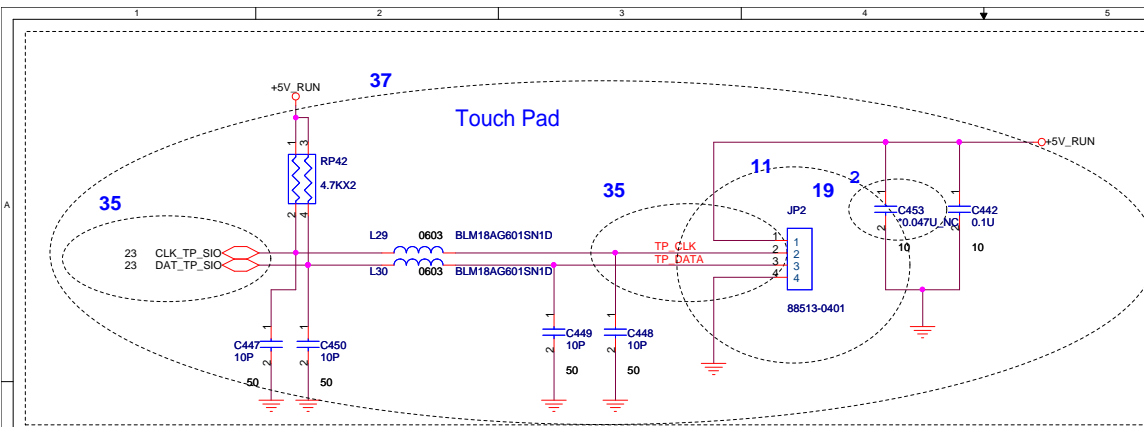


**QUANTA COMPUTER**

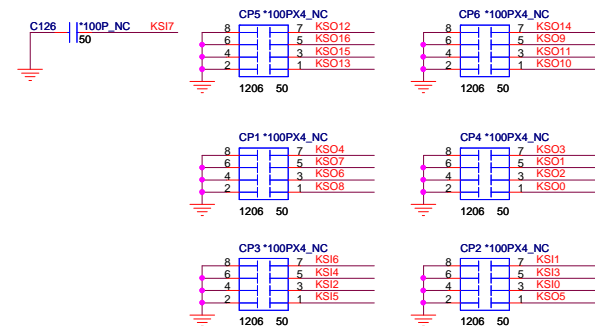
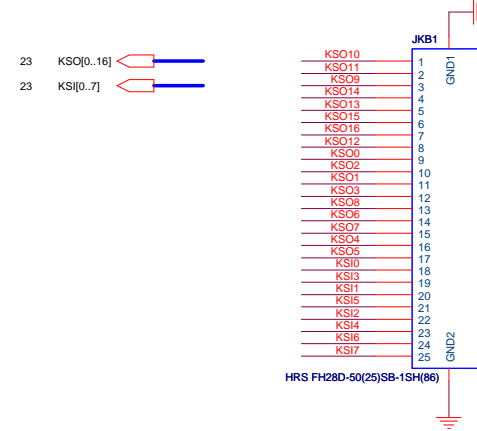
Title: SATA (HDD&CD\_ROM)

Size	Document Number	Rev
	VM9/VM8	1A

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### KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

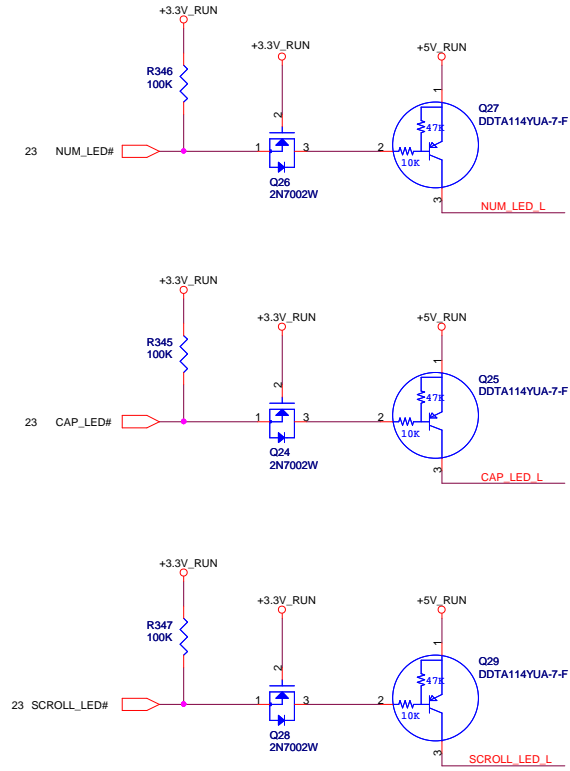
**QUANTA  
COMPUTER**

Title: TOUCH PAD, BULE TOOTH & FIR

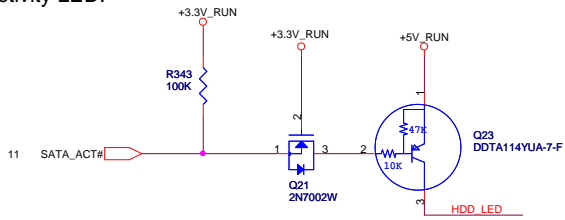
Size	Document Number VM9/VM8	Rev 1A
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Date: Tuesday, June 17, 2008      Sheet 29 of 53

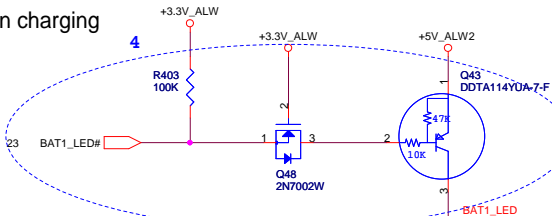
### Keyboard LED



### HDD activity LED.

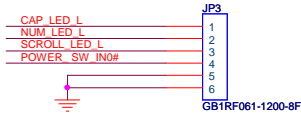


### Battery in charging

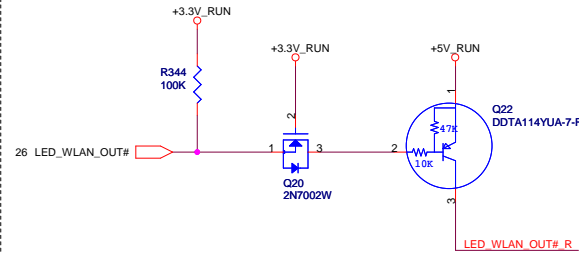


20

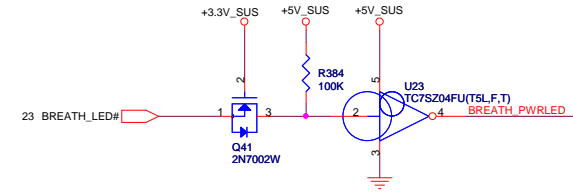
### Dash board connector



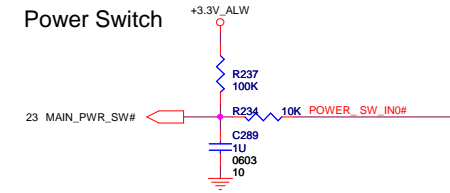
### WLAN



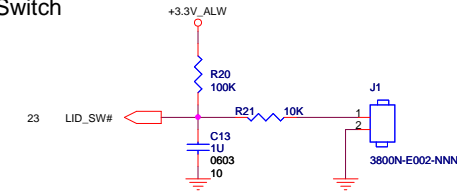
### Power & Suspend.



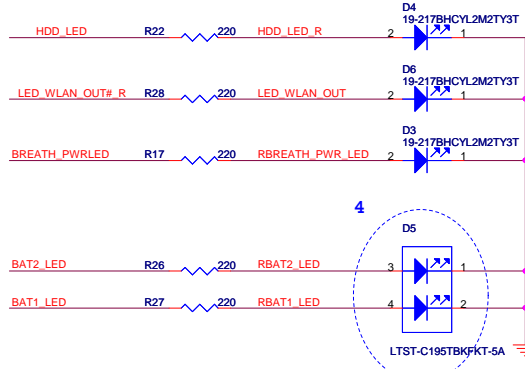
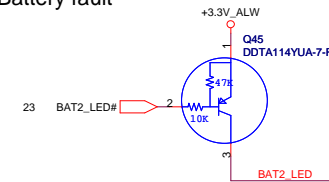
### Power Switch



### LID Switch



### Battery fault

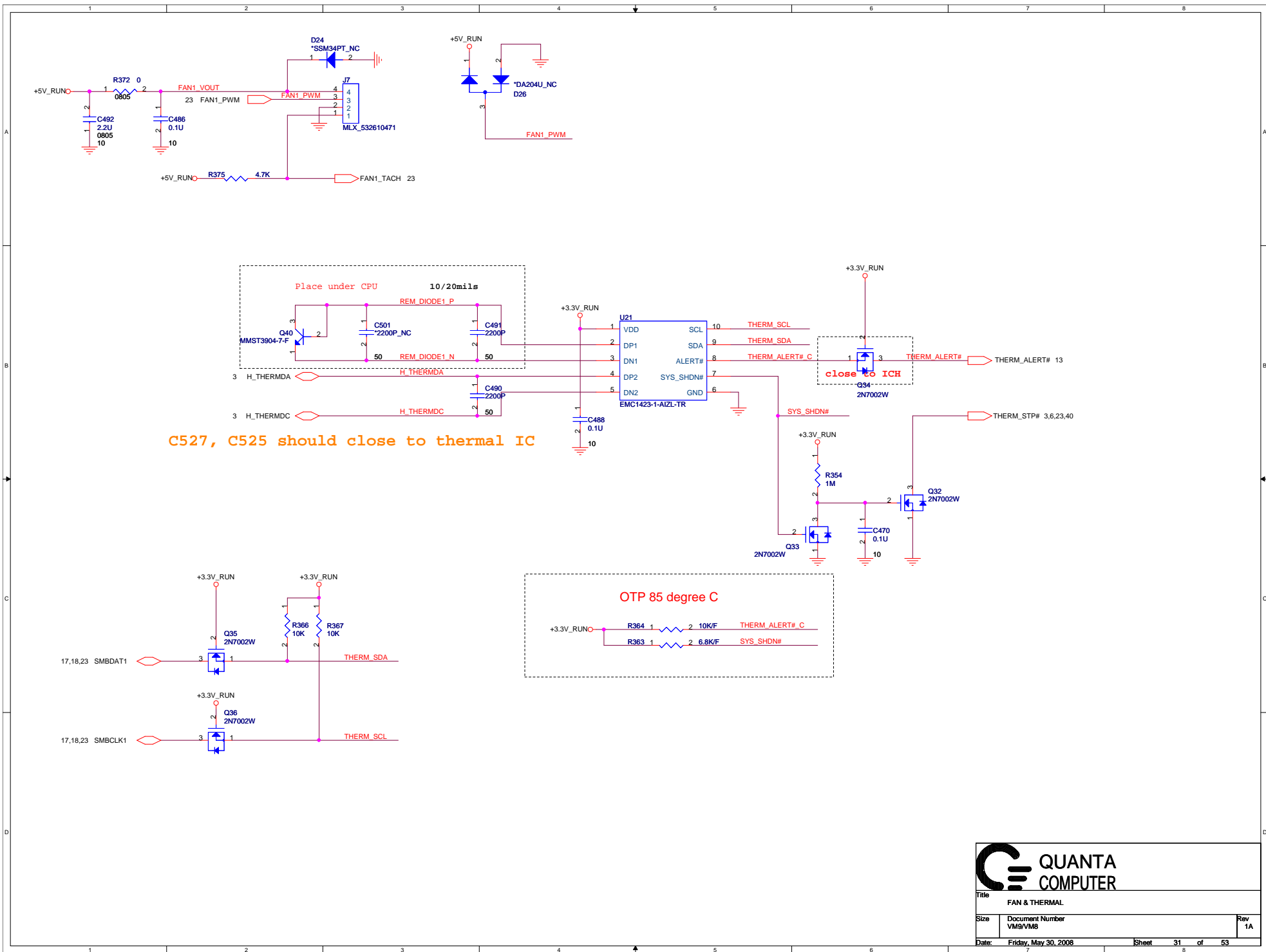


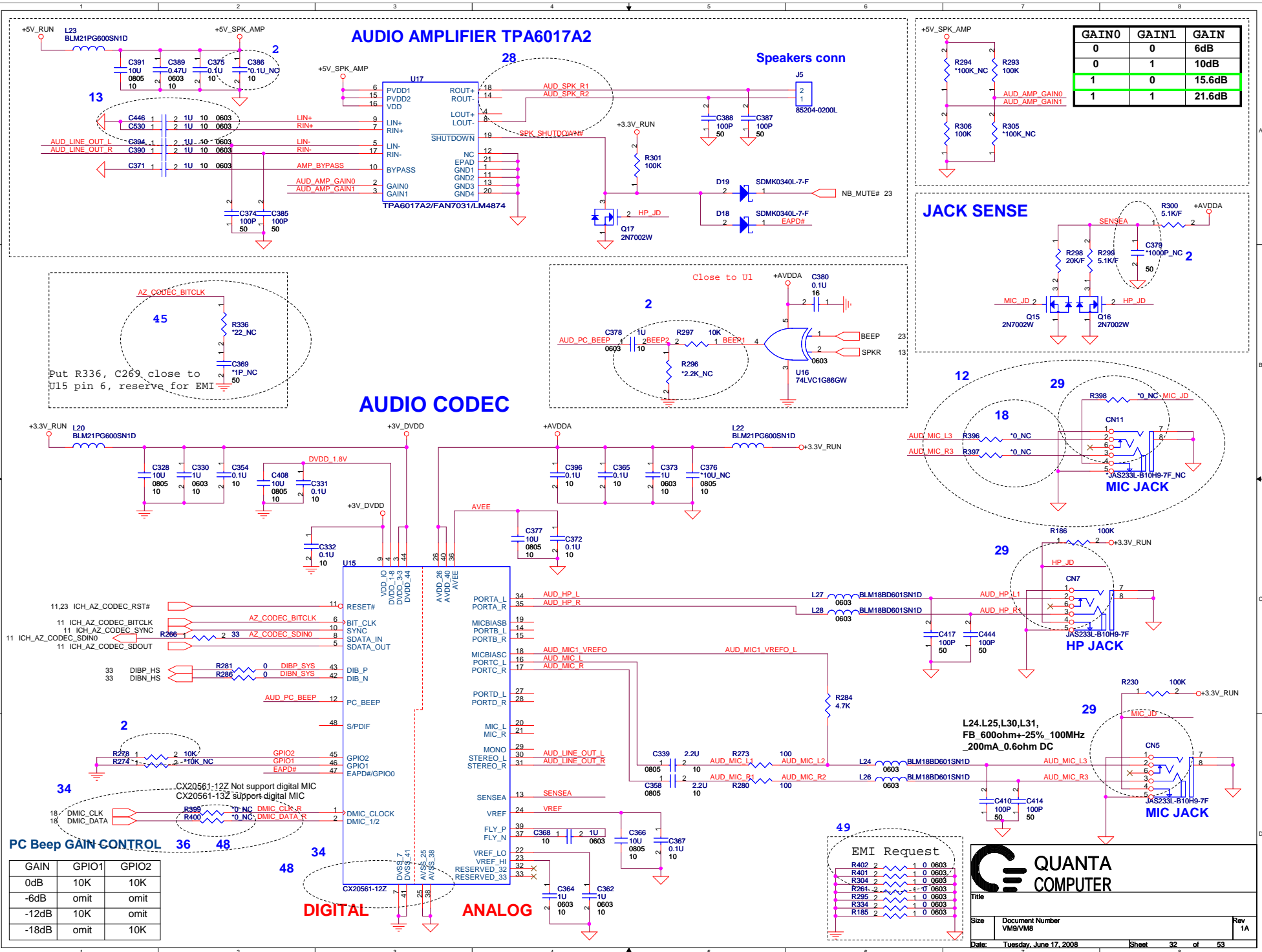
Title SWITCH, KEYBOARD & LED

Size Document Number VM9/VM8

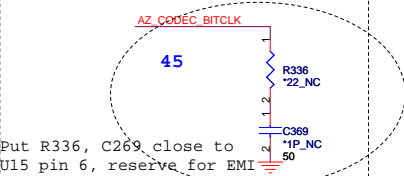
Rev 1A

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GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

**EMI Request**

R402	2	1	0	0603
R401	2	1	0	0603
R304	2	1	0	0603
R261	2	1	0	0603
R295	2	1	0	0603
R334	2	1	0	0603
R185	2	1	0	0603

**QUANTA COMPUTER**

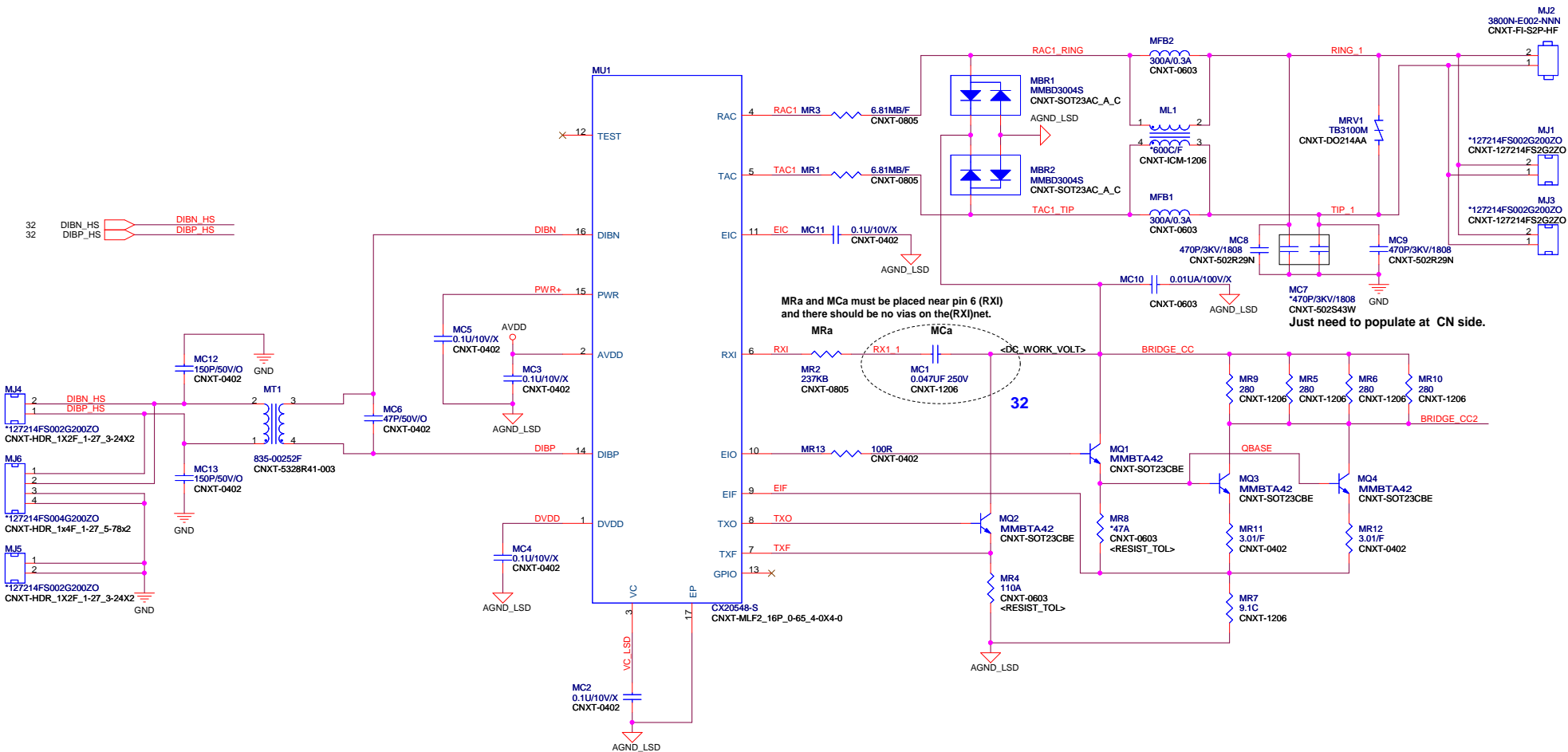
Title: \_\_\_\_\_

Size: \_\_\_\_\_ Document Number: VM9/VM8 Rev: 1A

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Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		

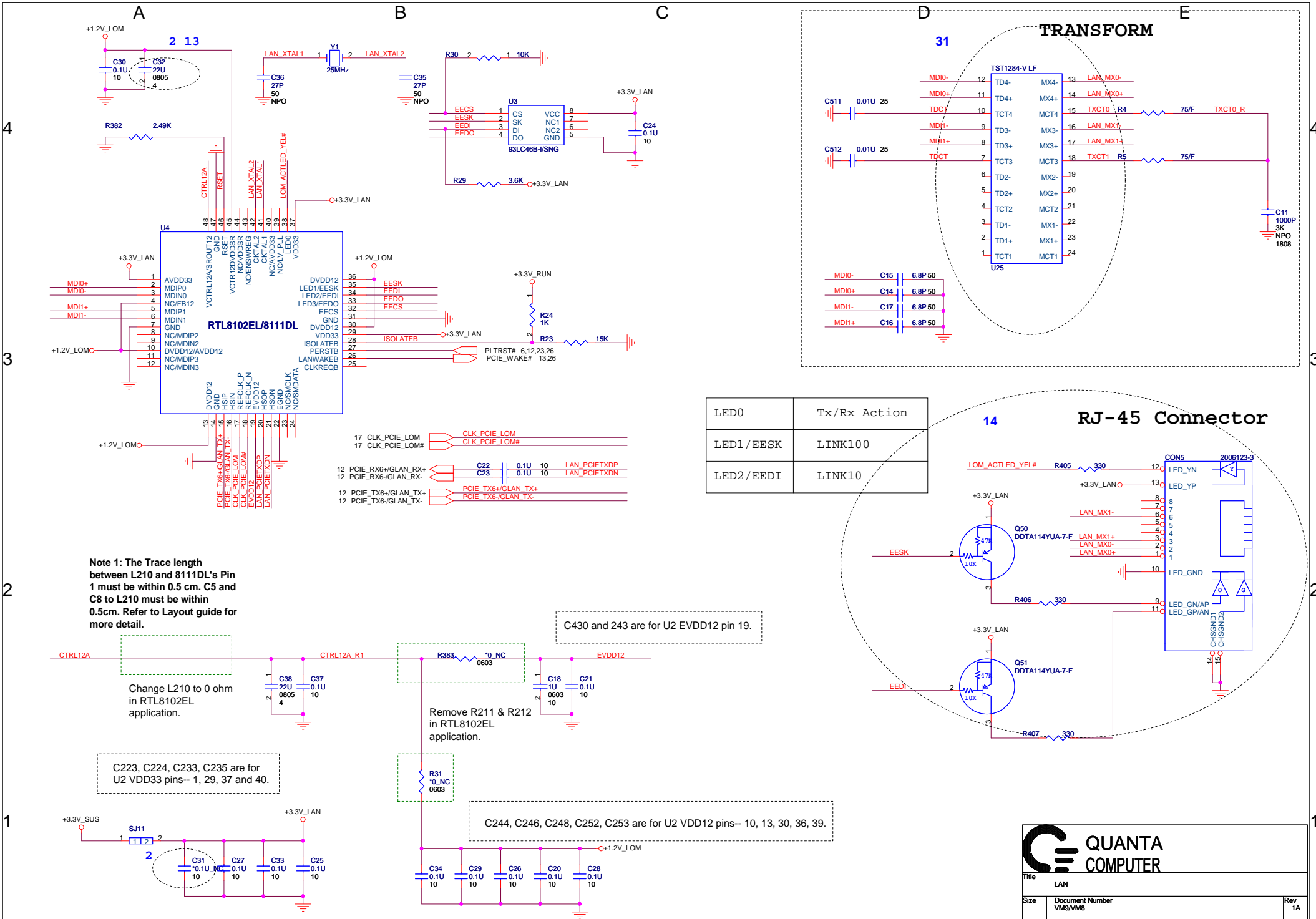


**QUANTA COMPUTER**

Title: \_\_\_\_\_

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**Note 1:** The Trace length between L210 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L210 must be within 0.5cm. Refer to Layout guide for more detail.

LED0	Tx/Rx Action
LED1/EESK	LINK100
LED2/EEDI	LINK10

C430 and 243 are for U2 EVDD12 pin 19.

Remove R211 & R212 in RTL8102EL application.

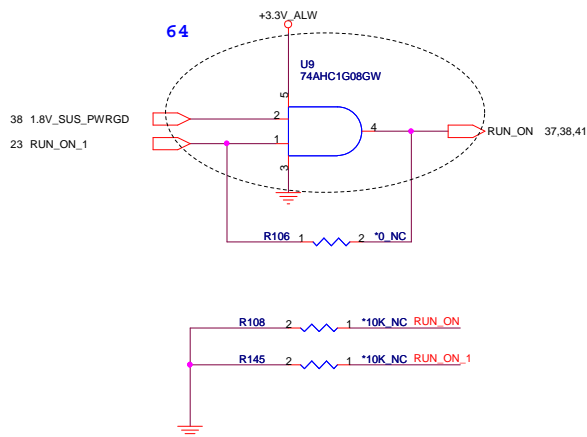
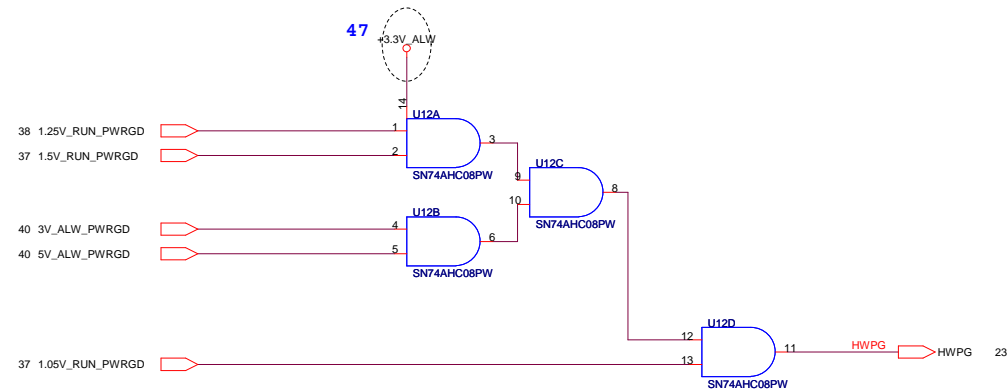
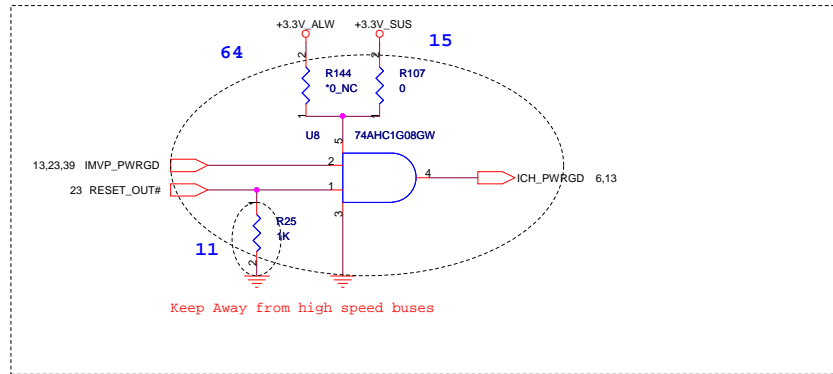
C244, C246, C248, C252, C253 are for U2 VDD12 pins-- 10, 13, 30, 36, 39.


Change L210 to 0 ohm in RTL8102EL application.

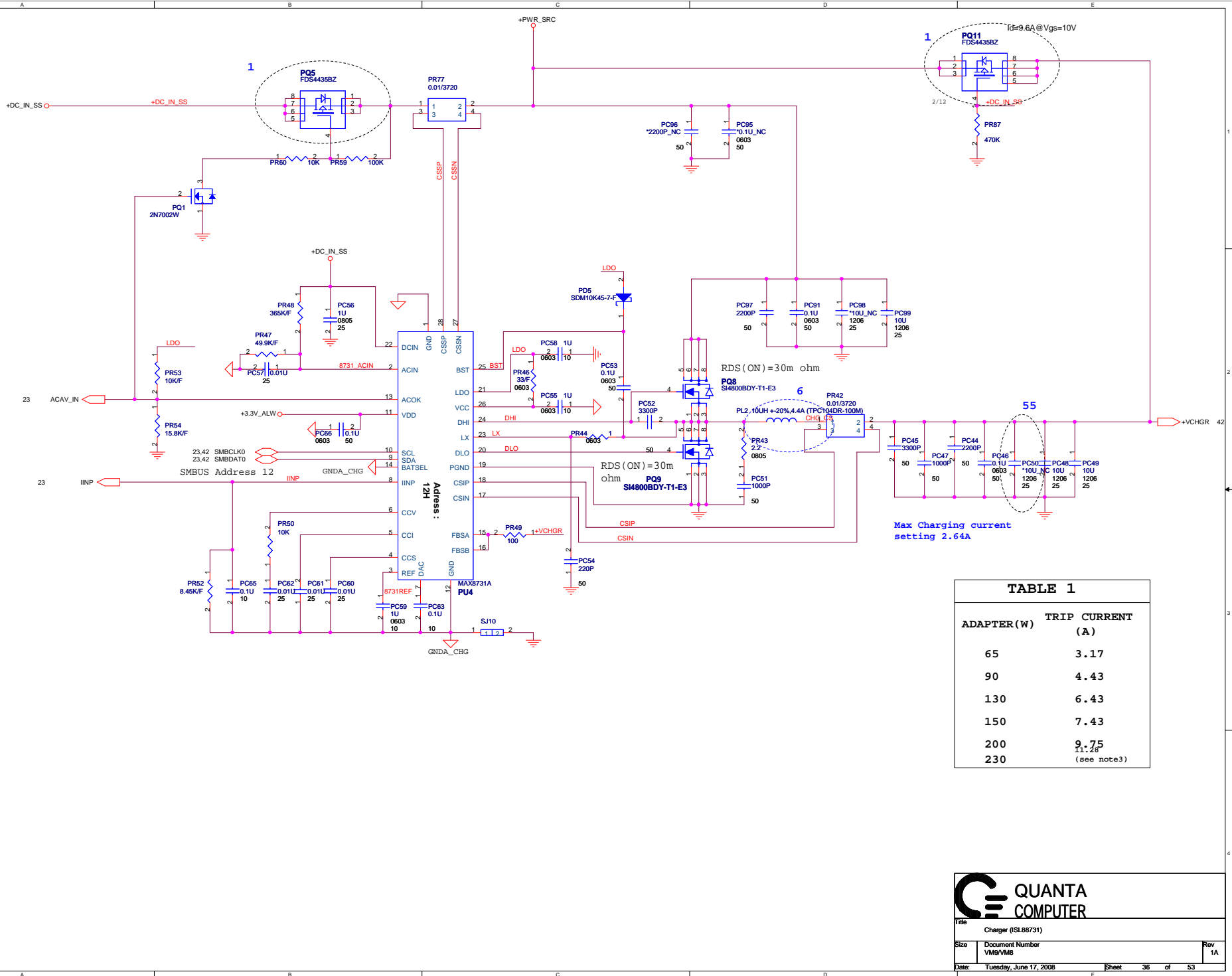
**QUANTA COMPUTER**

Title: LAN

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 <b>QUANTA COMPUTER</b>		Title	
		System Reset Circuit	
Size	Document Number	Rev	
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Max Charging current setting 2.64A

**TABLE 1**

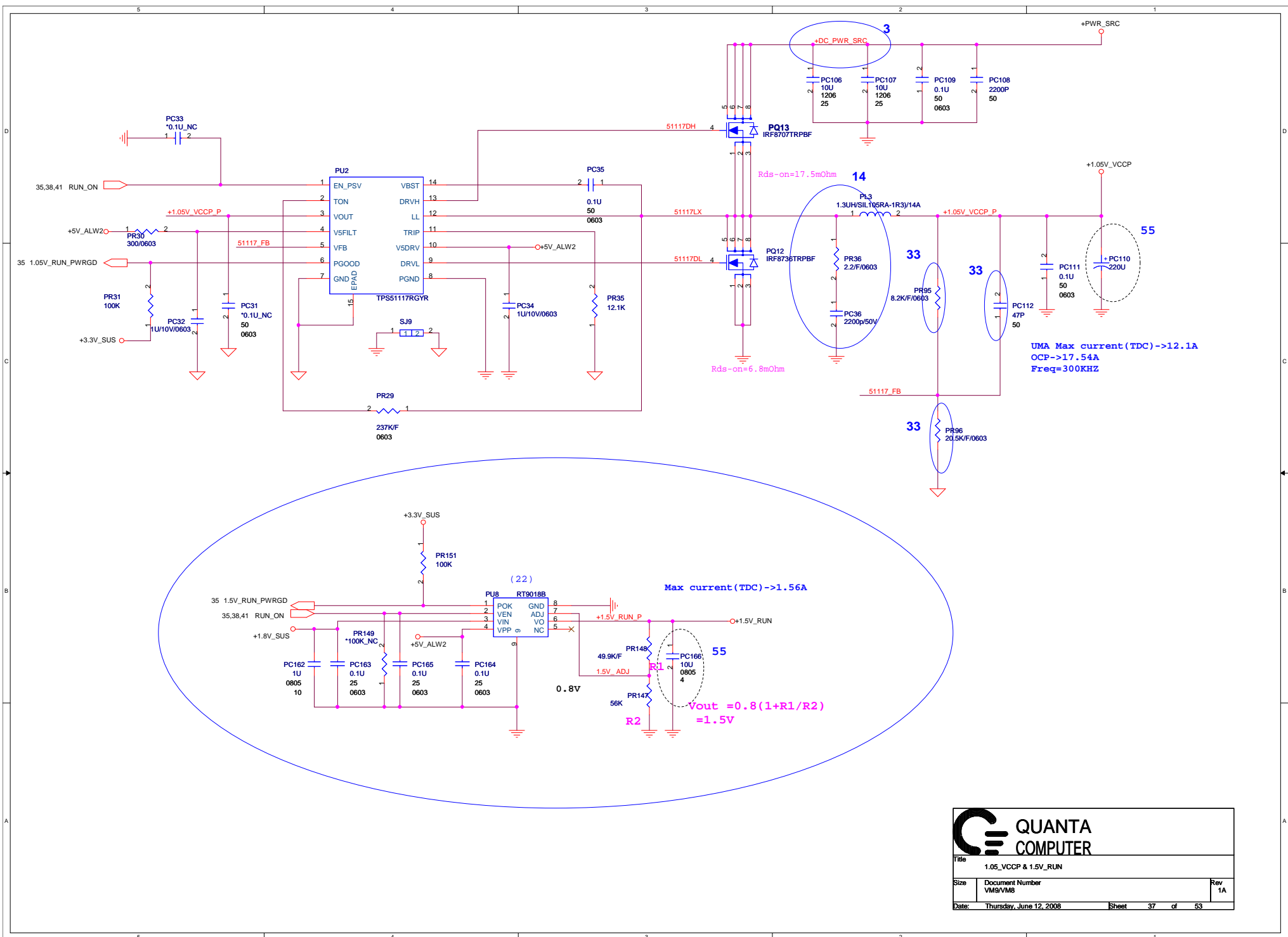
ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.26 (see note3)

**QUANTA COMPUTER**

Title: Charger (SL88731)

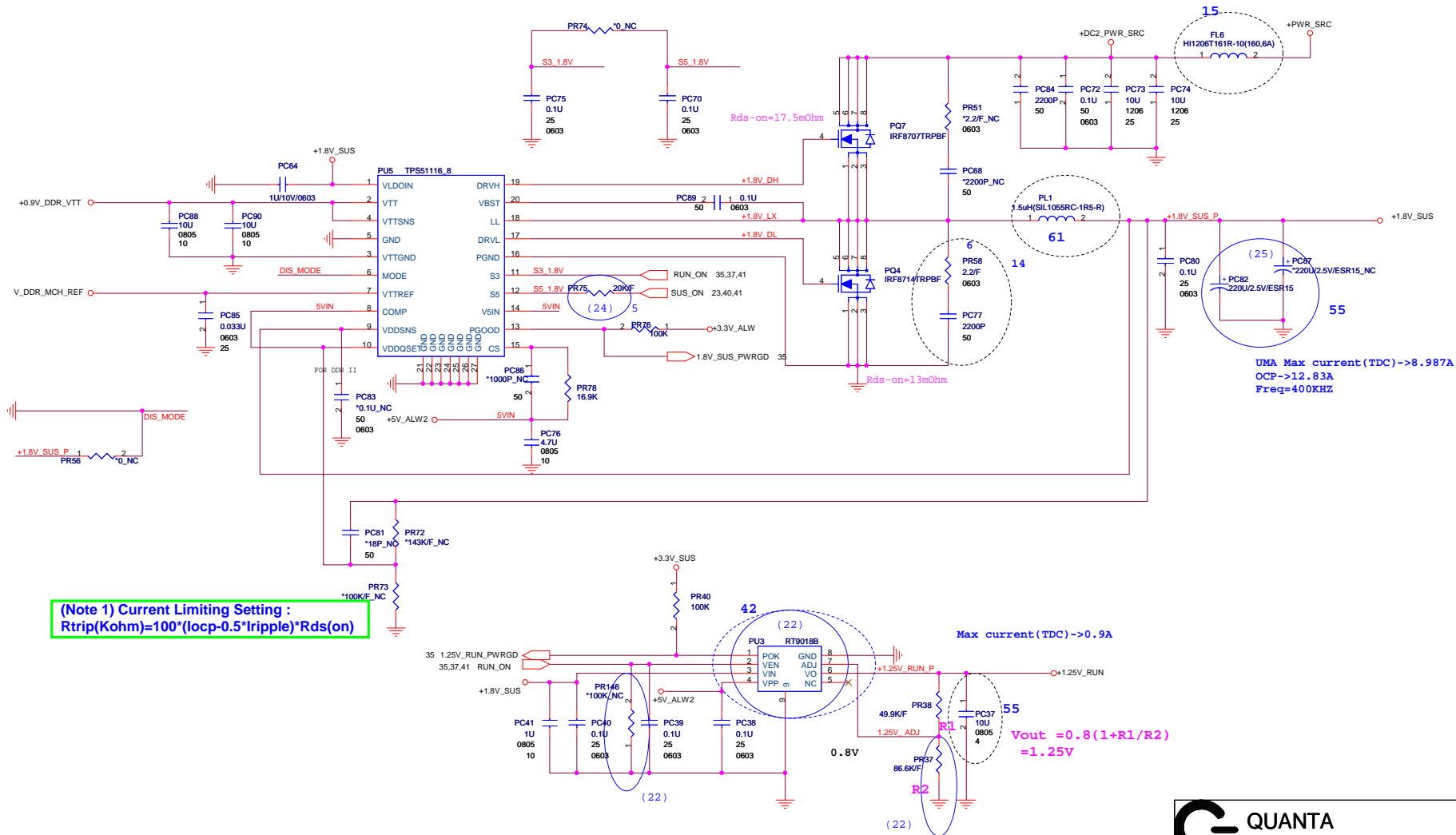
Size: Document Number VMS/VMS Rev: 1A

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**QUANTA COMPUTER**

Title: 1.05_VCCP & 1.5V_RUN		
Size: VM9/VM8	Document Number: VM9/VM8	Rev: 1A
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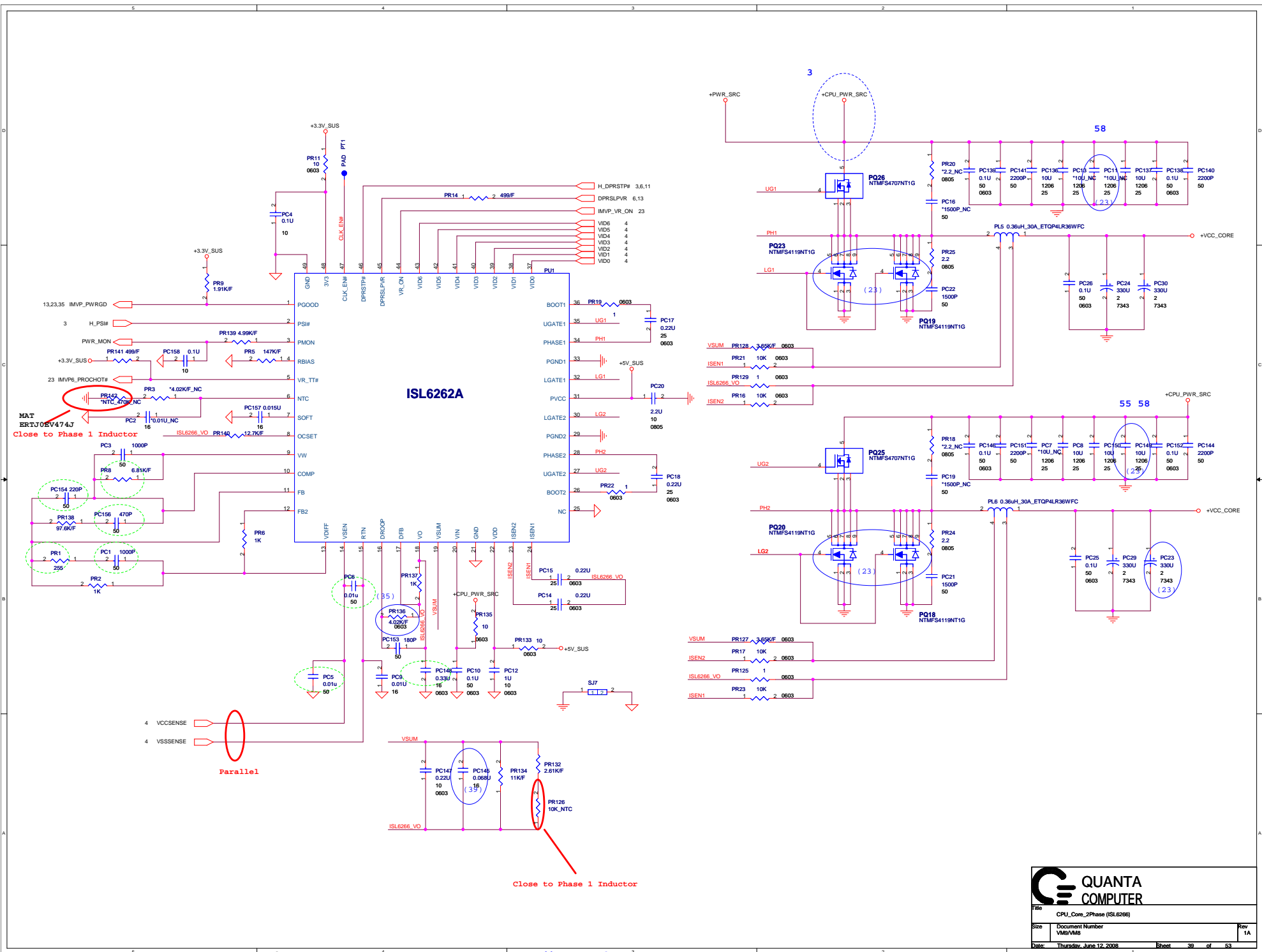
**(Note 1) Current Limiting Setting :**  
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{tripple}) * R_{ds(on)}$

Max current (TDC) -> 0.9A

UMA Max current (TDC) -> 8.987A  
 OCP -> 12.83A  
 Freq = 400KHZ

**QUANTA COMPUTER**

Title	1.8VSUS & 0.9VTT (TPS51116)		
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	VM9/VM8	1A	
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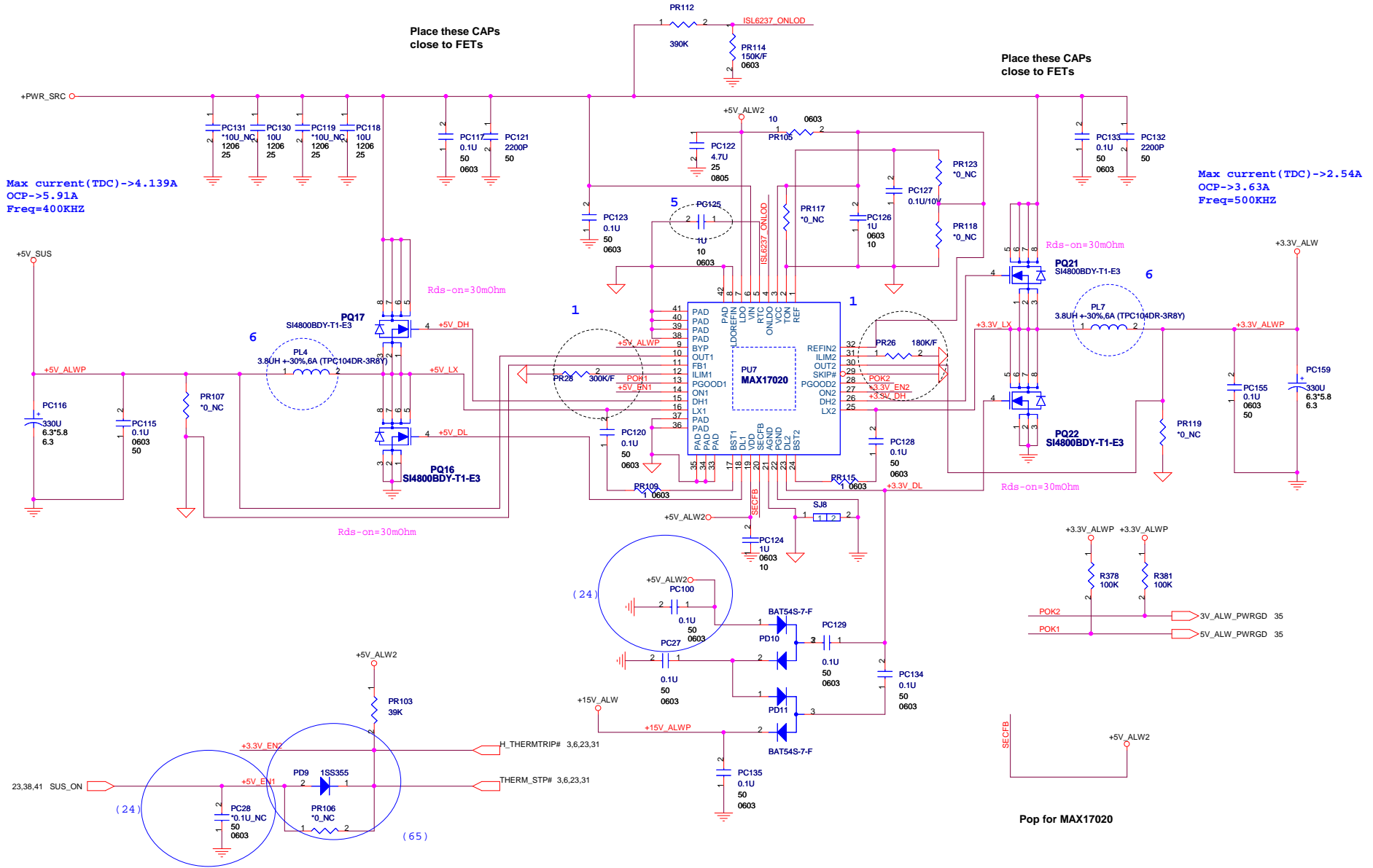


QUANTA COMPUTER	
Title CPU_Core_2Phase (ISL6266)	
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	Rev 1A

# DC/DC +3V\_ALW/+5V\_SUS/+5V\_ALW /+15V\_ALW

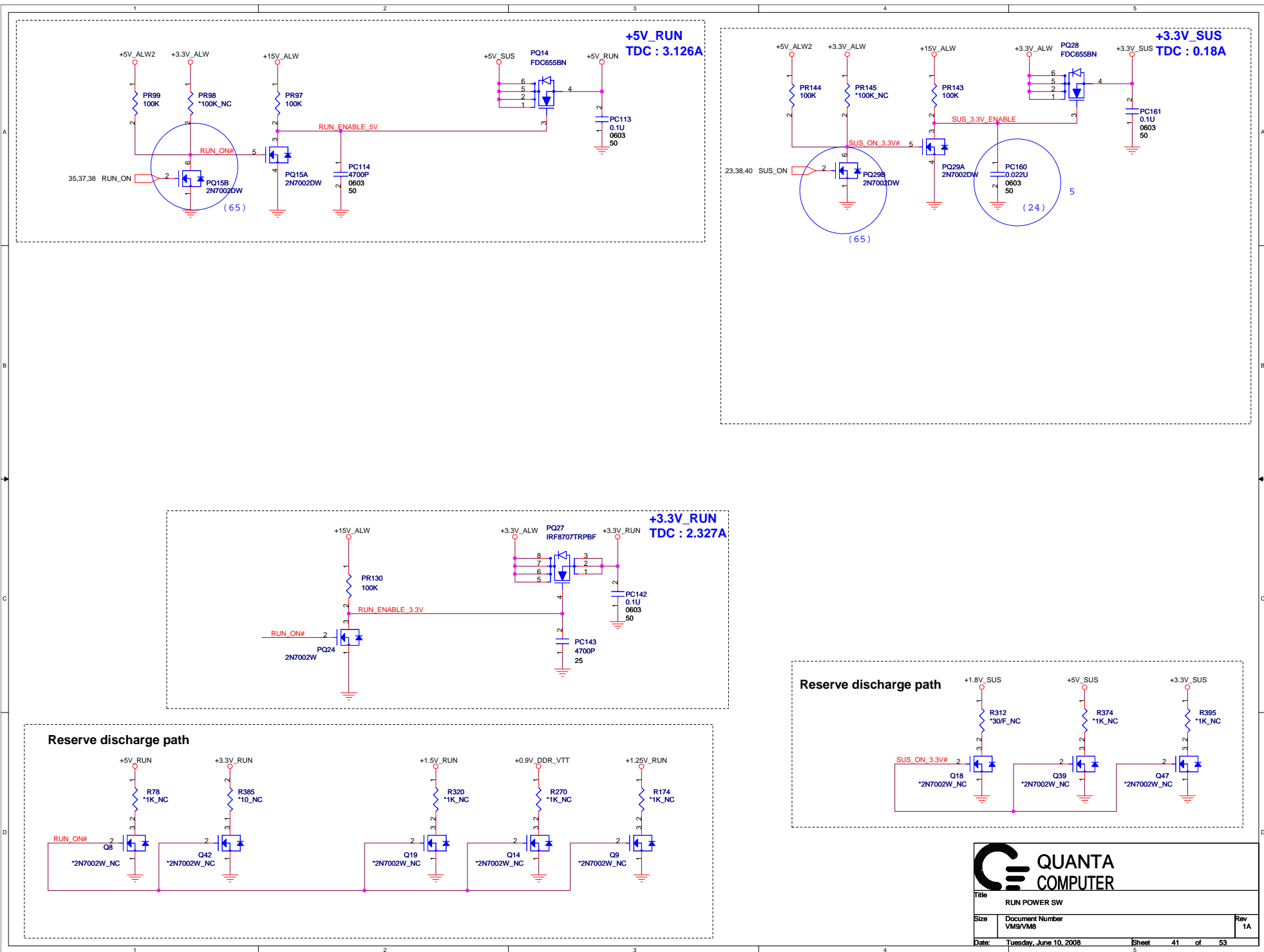
Place these CAPs close to FETs

Place these CAPs close to FETs

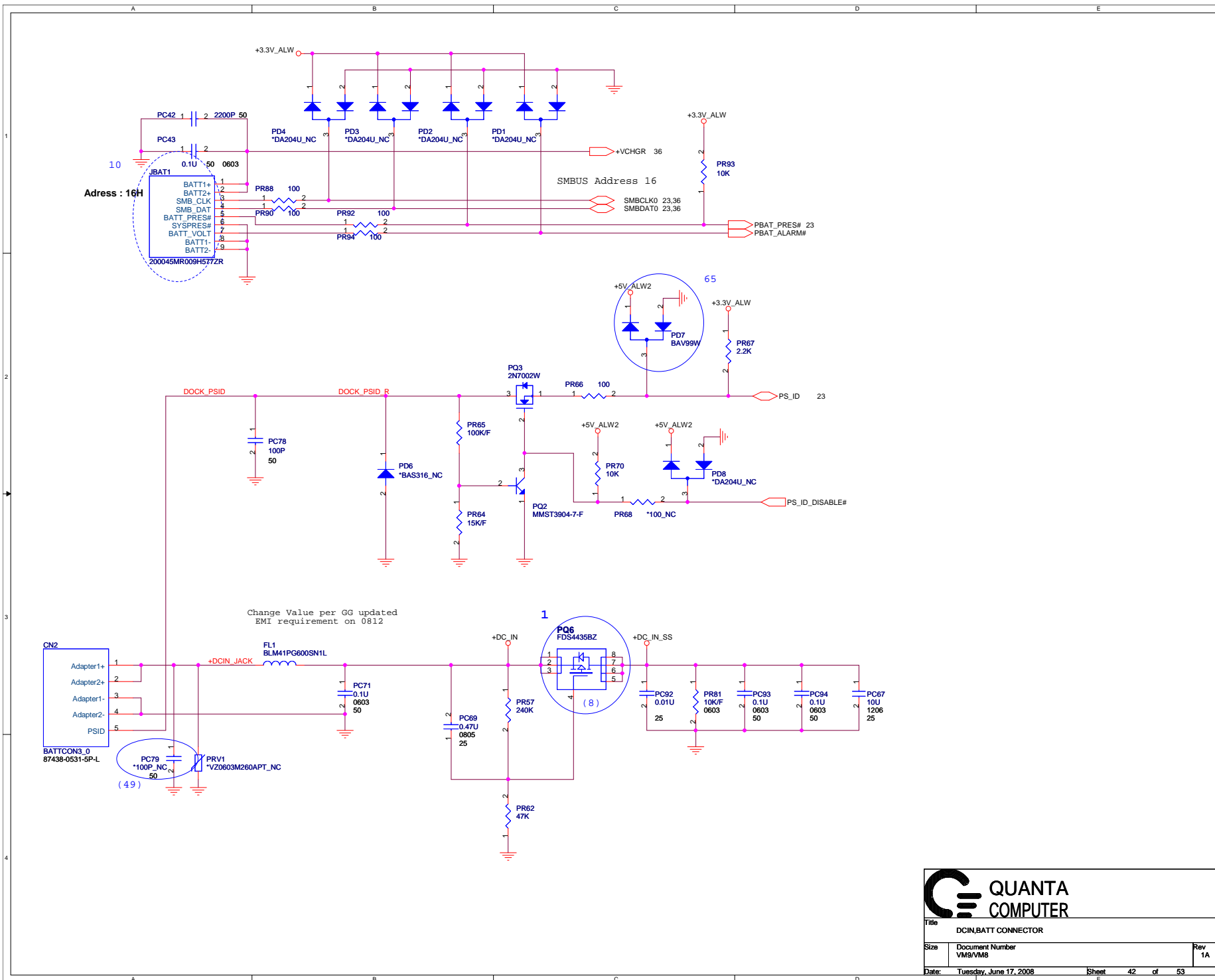


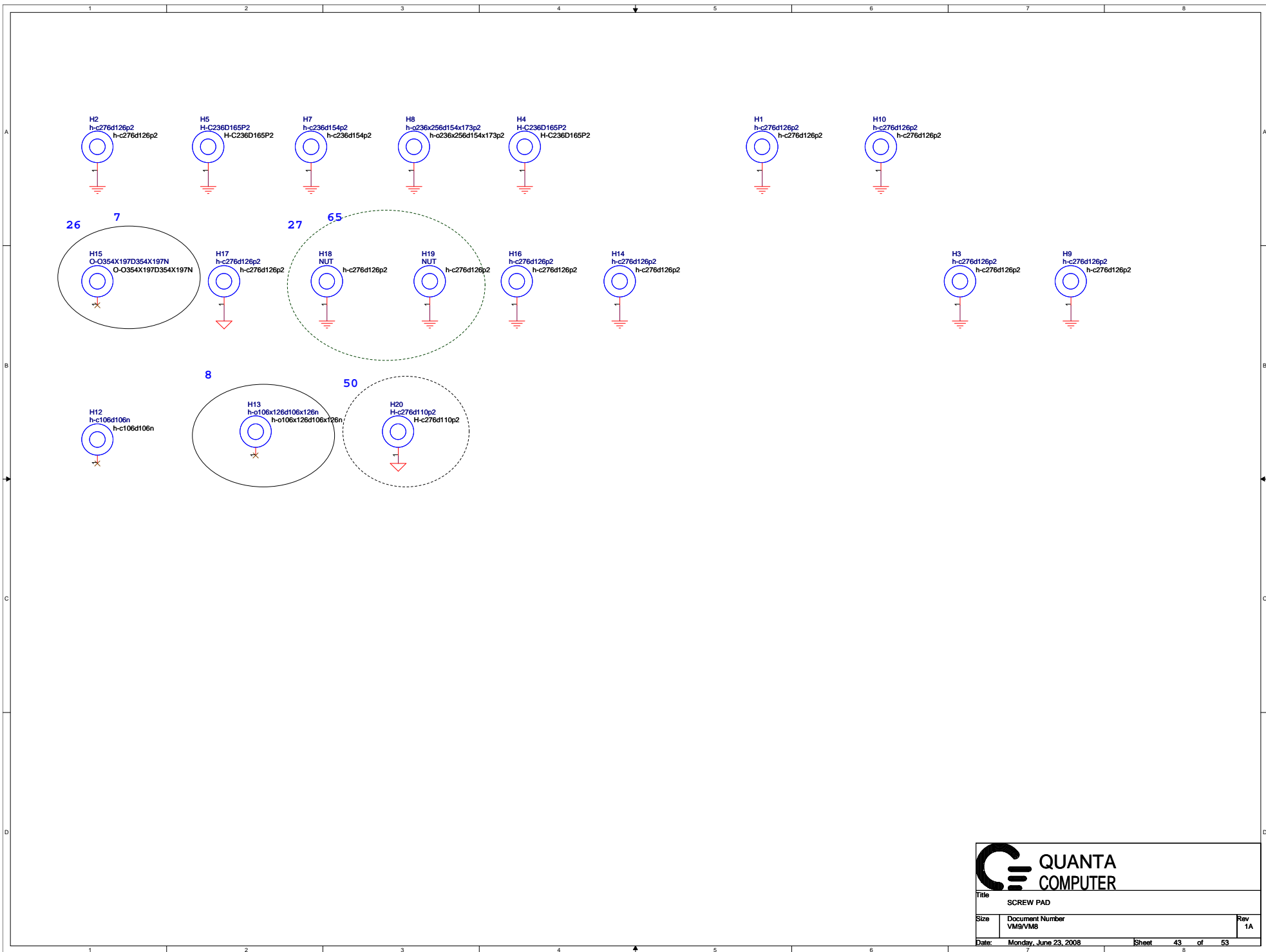
Title		
3VALW,5V,3V, Power On		
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Title			Rev
RUN POWER SW			1A
Size	Document Number		
	VM9/VM8		
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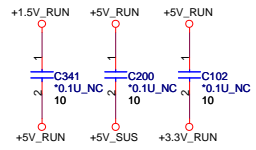




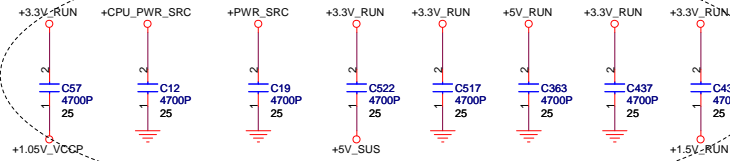
		<b>QUANTA COMPUTER</b>	
Title: SCREW PAD			
Size:	Document Number:	VM9/VM8	Rev: 1A
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Reserved for EMI.

Stitching caps for PCI bus.



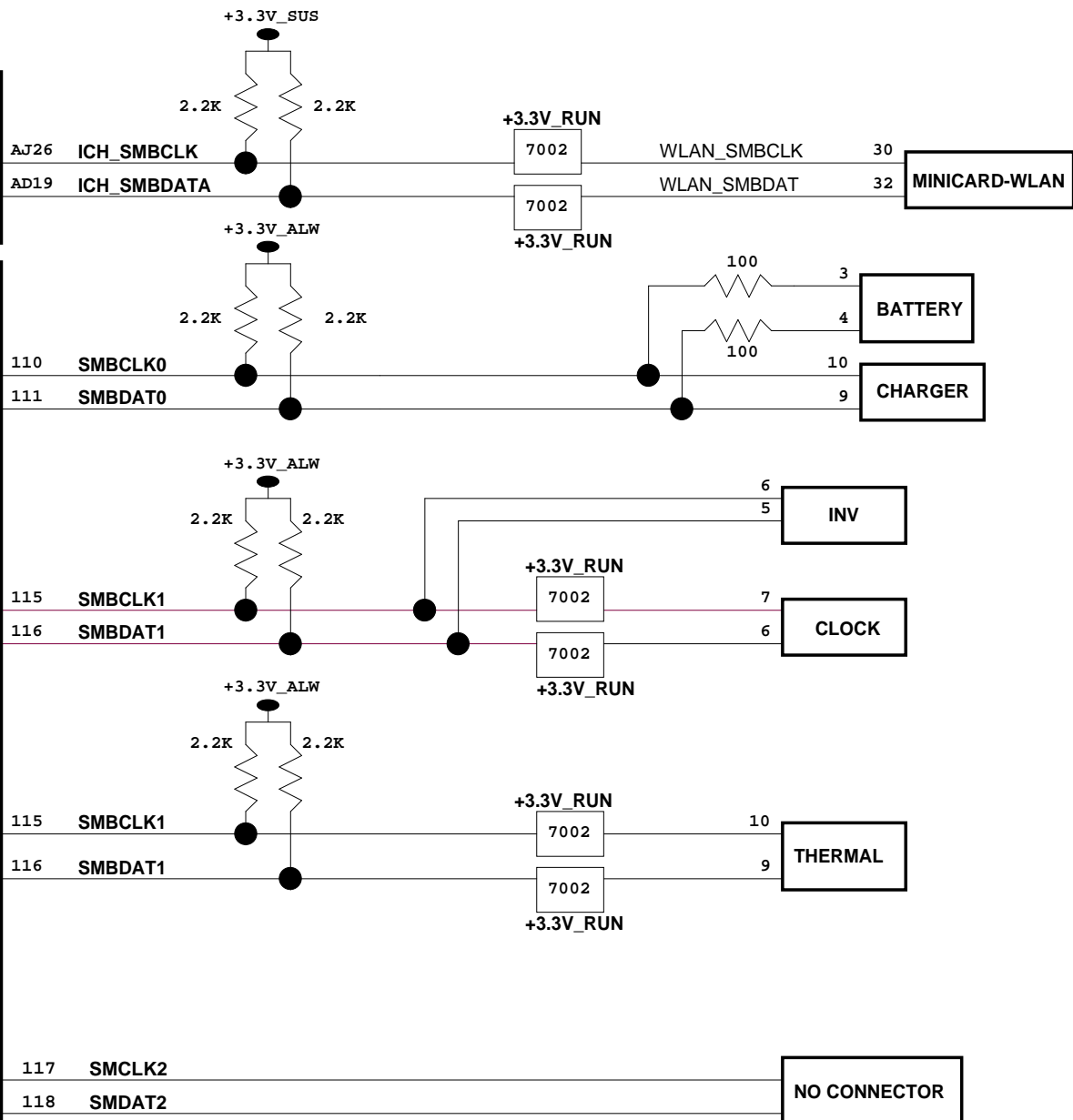
40 Stitching caps for PCI EMC.



Title		EMI CAP	
Size	Document Number	Rev	
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**ICH8-M**

**SIO  
ITE8512**

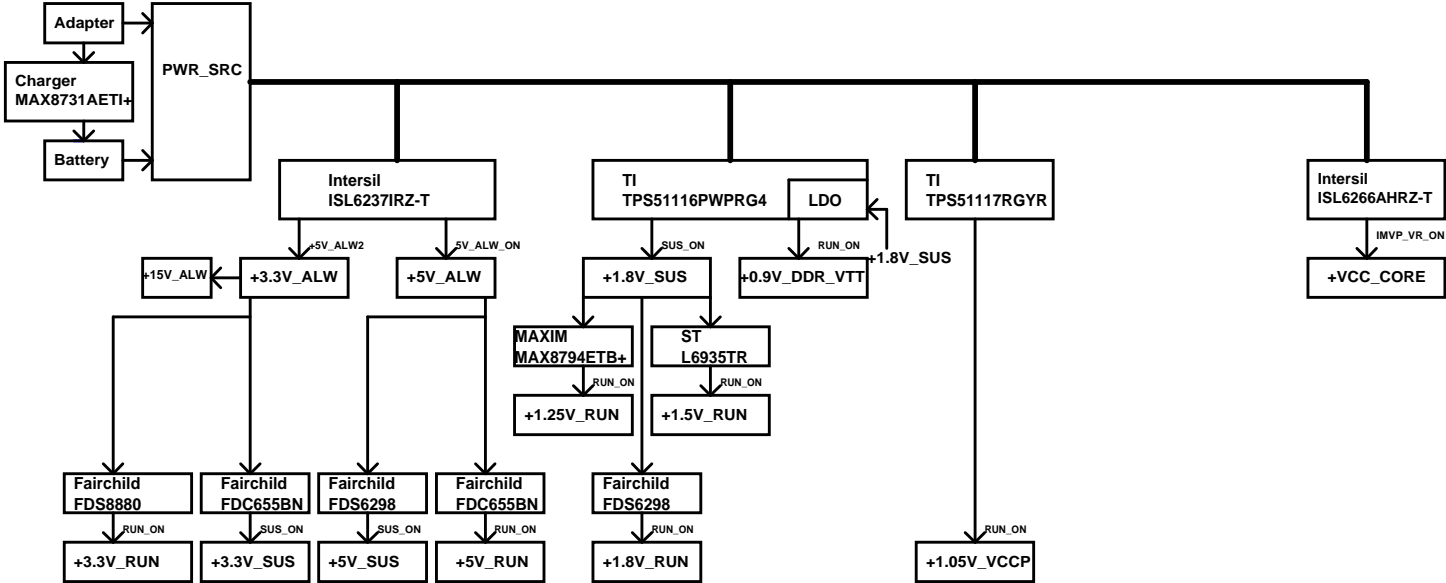



**QUANTA  
COMPUTER**

Title: SMBUS BLOCK

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 <b>QUANTA COMPUTER</b>	
File	Schematic Block Diagram1
Size	Document Number VMB/VMB
Date	Tuesday, May 27, 2008
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